Are the RISC-V Design Freedoms Leading to RISK in Verification Quality?

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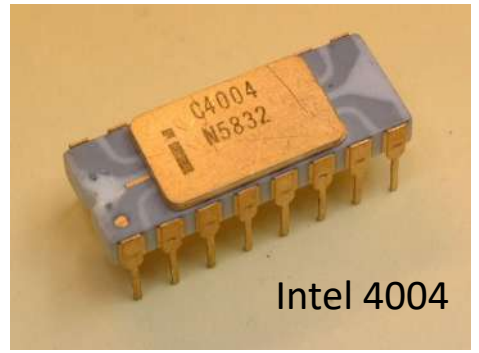
Imperas Story

- Imperas founding team has background in Electronic Design Automation (EDA) tools, and FPGA and processor IP companies
- Imperas founding team saw the need for tools and methodology similar to EDA for software debug, test and analysis, based on software simulation
- 5 years ago, Imperas saw that RISC-V was transitioning from an academic exercise to an industrial community
- After building processor models and tools to support more than 12 different instruction set architectures, jumping into RISC-V was a natural move for Imperas
- While design verification was not our first thought, it has become apparent – ***because customers have shouted this at us!*** – that RISC-V processor DV is on the critical path for broad RISC-V adoption

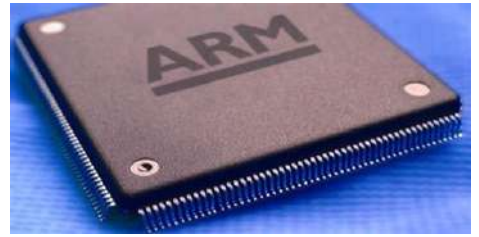
ISAs Past, Present & Future

- Earlier this year we marked 50 years since the invention of the microprocessor
- Intel and the x86 architecture has dominated the compute space for the last 40 years



Intel 4004

- Arm has dominated the mobile space for the last 20 years



- RISC-V? Poised to dominate all the unclaimed markets for the next 20/30/40 years

How Did Intel & Arm Come to Dominate Their Market Segments?

- Early entry
- Product met/exceeded the market requirements and expectations
- Ecosystem
- Quality product

What is RISC-V? Can RISC-V duplicate the business and technical conditions to dominate the unclaimed market segments?

What is RISC-V?

- It’s an instruction set architecture standard

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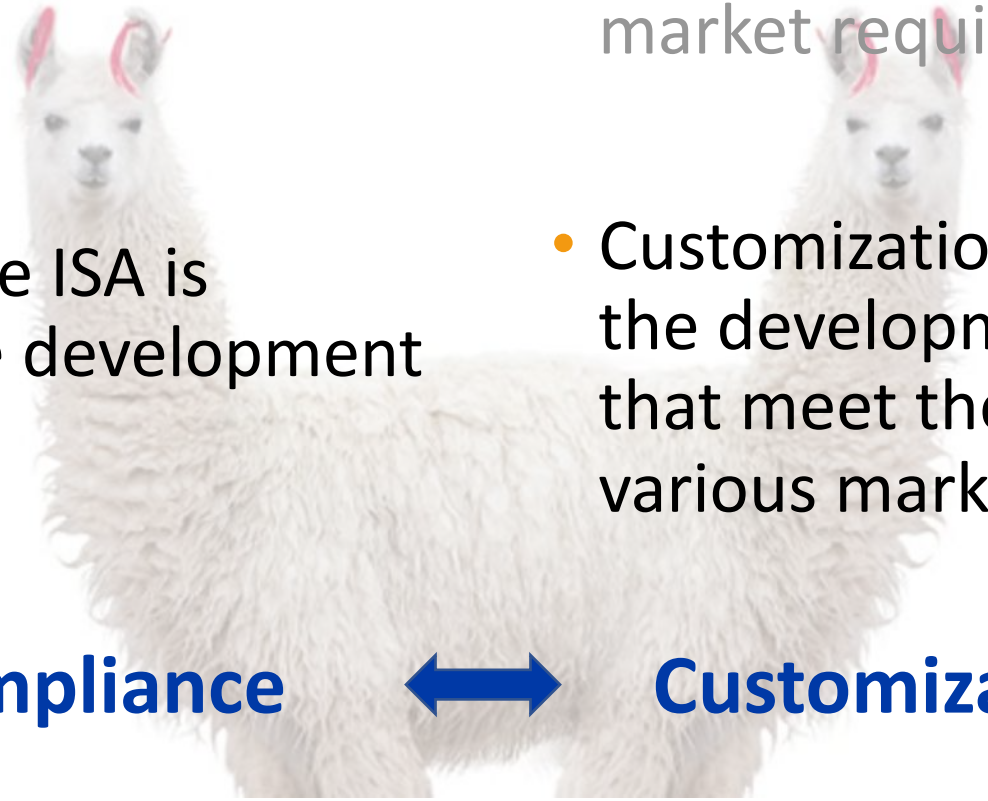
RISC-V is a Pushme-Pullyou Between Compliance and Customization

- It's an instruction set architecture standard
- Compliance to the ISA is important for the development of the ecosystem
- It's the ability to customize a processor to meet specific market requirements
- Customization is important for the development of products that meet the demands of the various markets



Compliance ⟷ **Customization**

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What is RISC-V? Can RISC-V duplicate the business and technical conditions to dominate the unclaimed market segments?

How Did Intel & Arm Come to Dominate Their Market Segments?

- Early entry – depends on the business using RISC-V, and the market they are attacking

✓ Product met/exceeded the market requirements and expectations

✓ Ecosystem

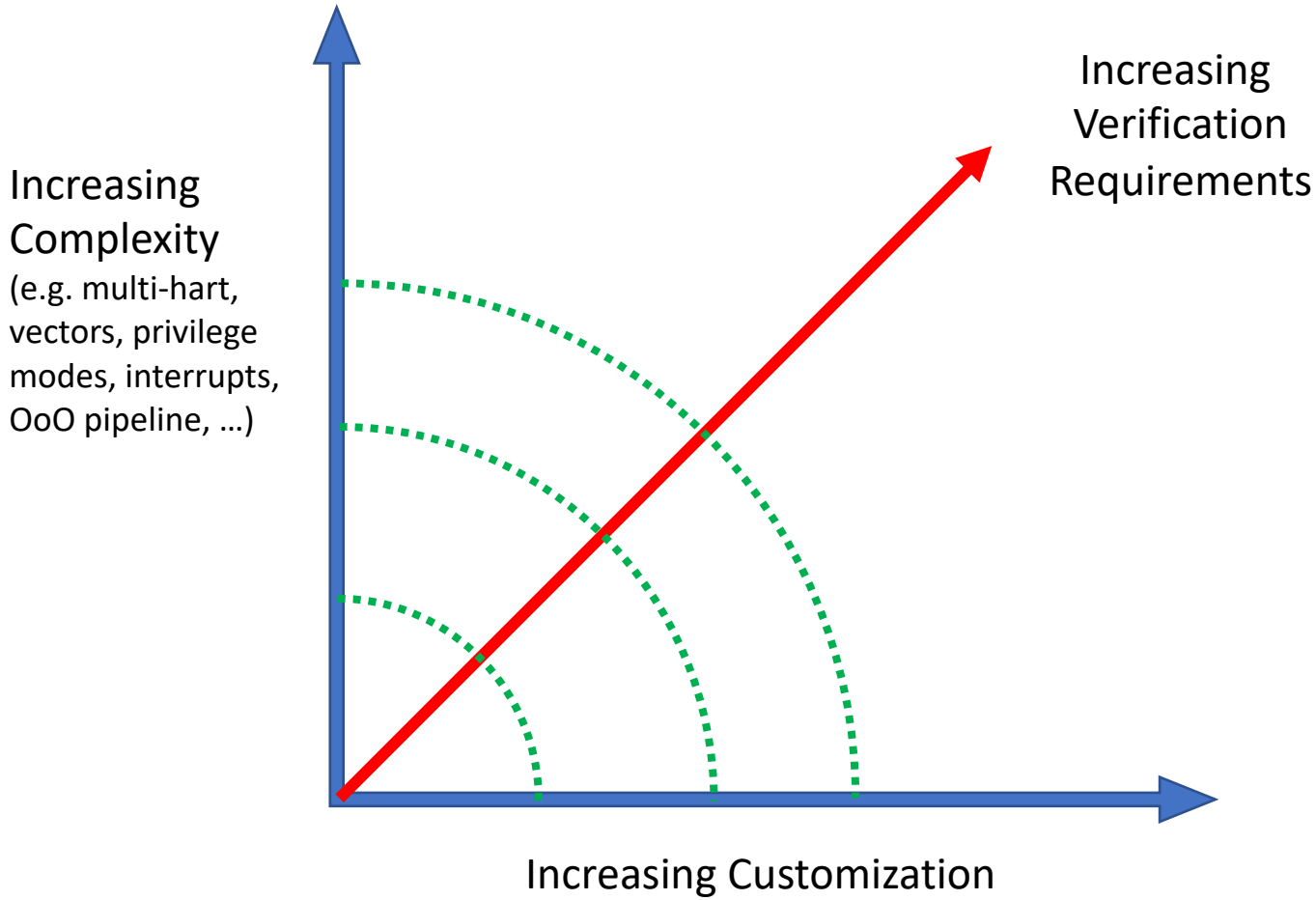
- Quality product

The Critical Element for RISC-V Worldwide Domination is Product Quality, i.e. RISC-V Processor Design Verification

Quality Product = Comprehensive DV Effort

- DV history: 20+ years ago the EDA industry collaborated with semiconductor companies to develop verification tools and methodology for SoC DV, helping customers achieve over 90% first silicon success, versus the industry average of 40%
- However, verifying SoC blocks and a complete SoC is different from verifying a CPU
  - Intel, Arm and others have kept verification in house; best known methods are not public
  - However, DV engineers from these companies are now taking jobs in the RISC-V community; SiFive and Codasip are good examples of adding processor DV teams
  - Processor IP companies that were previously supporting their own ISAs – e.g. Andes, MIPS – are now part of the RISC-V community

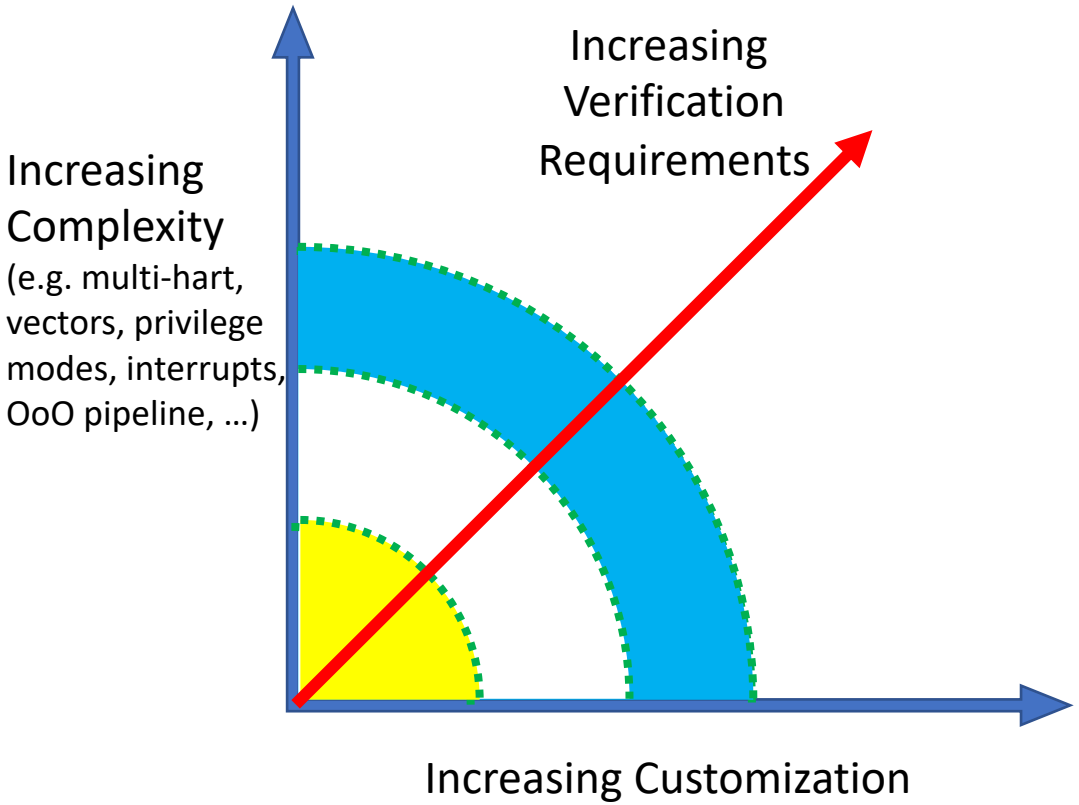
RISC-V DV Requirements



Processor DV Is Not SoC DV

- Some commonalities
  - Still want to use UVM
  - Still want to use constrained random test generation ("instruction stream generation")
  - Still want to have functional coverage metrics
  - However …
- A Reference Model is needed for checking correct behavior
- Advanced processor features – *multiple harts, interrupts, privilege modes, Debug mode, multi-issue and out-of-order pipelines, …* – make the DV requirements much more demanding

RISC-V DV Requirements

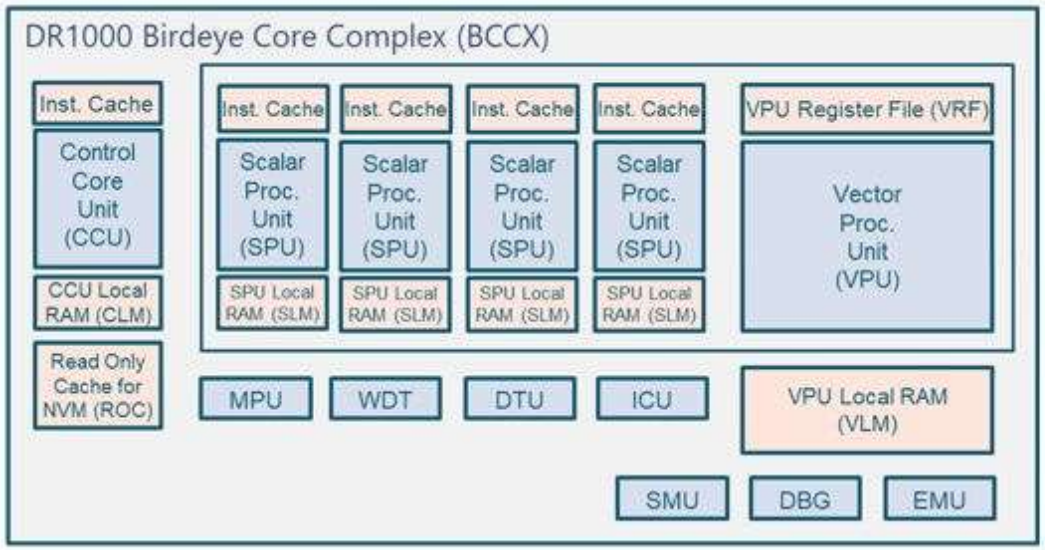


- At the low end, post-simulation trace-compare methodology will usually work
- At the high end, asynchronous-step-compare methodology is needed
- Imperas, and our customers and partners, are working together to develop and publicize RISC-V DV methodology
  - Nagravision, NSITEXE, Nvidia Networking, Silicon Labs, …
  - Andes, Codasip, MIPS, OpenHW Group, SiFive, …

imperas

Hello, my name is Koji Adachi from NSITEXE,
I am the manager of RISC-V core development.
NSITEXE is a subsidiary of DENSO, our knowledge is automotive electronic devices.
For over 2 years NSITEXE has been been developing
multiple-hart vector RISC-V processors with Imperas.
As for this years news, our first product, DR1000C has received ISO 26262 ASIL-D ready certification.
And now we have done a big deal with the most famous automotive IC vendor.
We have already started a new core project with Imperas DV.
The new core is a more challenging and difficult development
and I expect Imperas DV technology to deliver the most high performance and high quality.

NSI-TEXE



MPU: Memory Protection Unit
WDT: Watch Dog Timer
DTU: Data Transfer Unit
ICU: Interrupt Controller/Request

SMU: System Management Unit
DBG: Debug Unit
EMU: Error Management Unit

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- 2021-Jul-13
  - NSITEXE achieves world's first RISC-V processor with vector extension certified for ***ISO 26262 ASIL D*** ready product
- 2021-Aug02
  - NSITEXE: A New product RISC-V 32bit CPU "NS31A" which supports ***ISO26262 ASIL D***
- 2021-Nov-09
  - NSITEXE DR1000C, a RISC-V based parallel processor IP with vector extension (DFP: Data Flow Processor) has been ***licensed for Renesas' new RH850***/U2B Automotive MCUs

Imperas and RISC-V DV

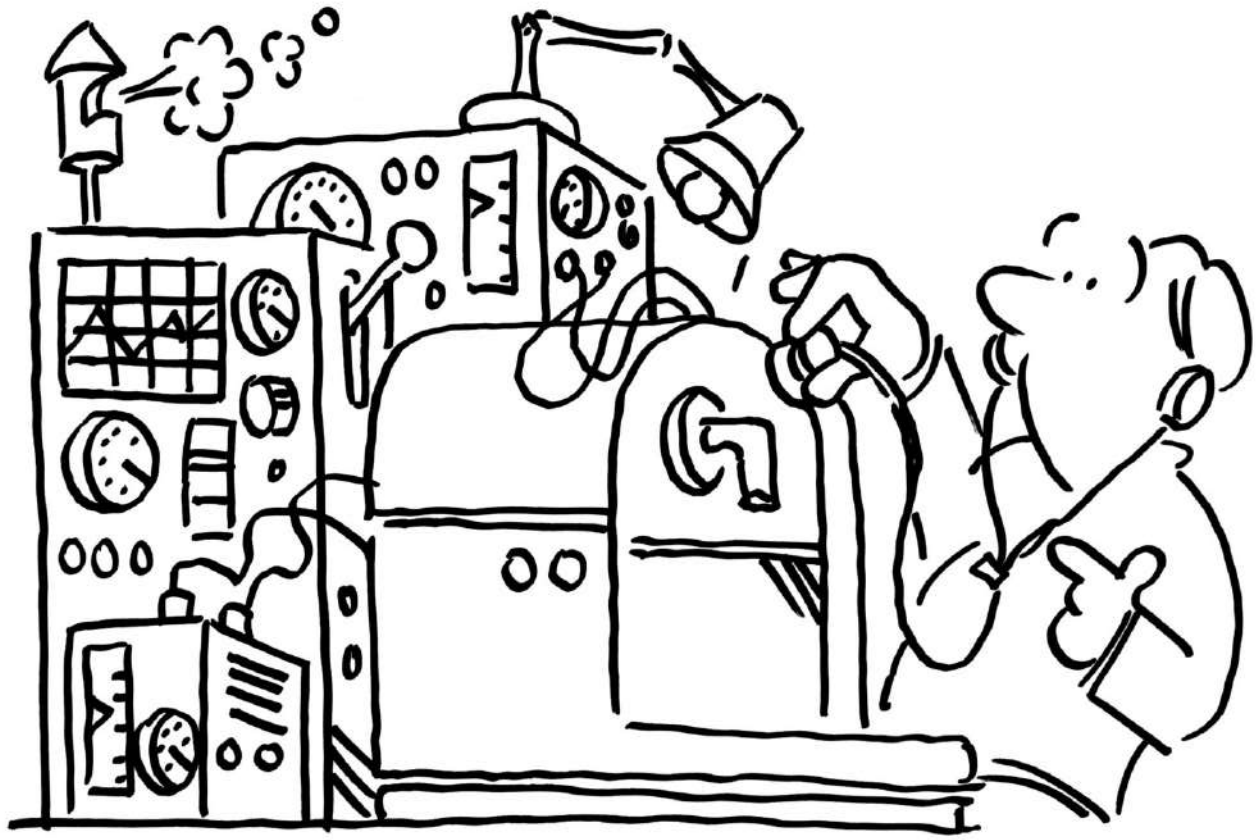
- Working on models since 2016
- Working on compliance since 2017
- Working with customers on RISC-V DV since 2018
- Evolving levels of DV

- **Announced today: ImperasDV solutions for RISC-V processor DV**

RISK in RISC-V?

- **RISK** can be reduced to **risk** by deploying a well thought out verification methodology, including production-proven tools and reference models

- ImperasDV solutions
  - Come to our booth!
  - www.imperas.com



Thank you

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For more information on ImperasDV stop by our RISC-V Booth or visit

www.imperas.com/ImperasDV