Virtual Platforms, Simulators and Software Tools

DAC – San Francisco
June 2018

Simon Davidmann – Imperas Software Ltd

Agenda

- Introduction to Imperas

- Embedded Software Development Challenges
- Range of Models and Solutions

- Recent News

Introduction to Imperas

- Founded 2008
  - Background: Verilog, VCS, Verisity, Exemplar, Arm, MIPS
- Focus on simulation, modeling, tools for embedded software developers
- Provide solutions for simulation of platforms to develop software on

imperas

"nobody designs a chip without simulating it, and we believe that nobody should be developing embedded software without simulating it"

Imperas Summary

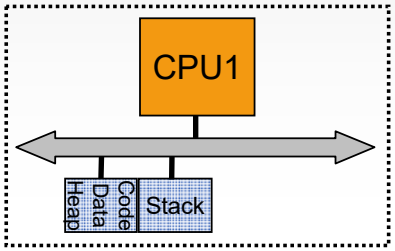
- Enable users to reduce embedded software schedules; improve software quality; achieve reliability, safety and security requirements; mesh with modern development methodologies such as Agile and Continuous Integration

- Key technologies
  - Instruction accurate simulation engines
  - Processor modeling methodology and library
  - Platform modeling methodology and library
  - Software development, debug, test and analysis tools

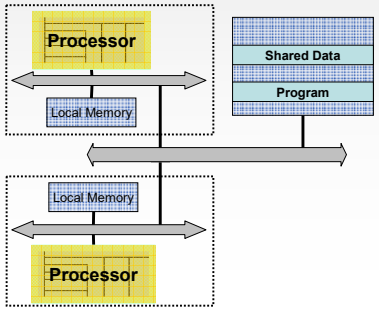
Agenda

- Introduction to Imperas
- Embedded Software Development Challenges
- Range of Models and Solutions
- Recent News

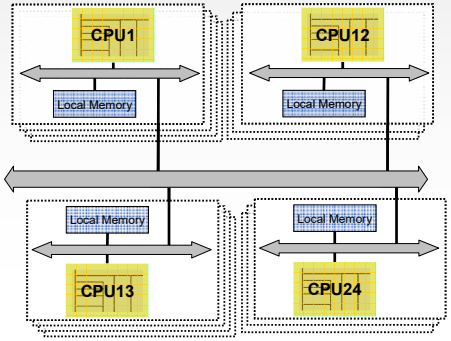
Processor Platform Configurations



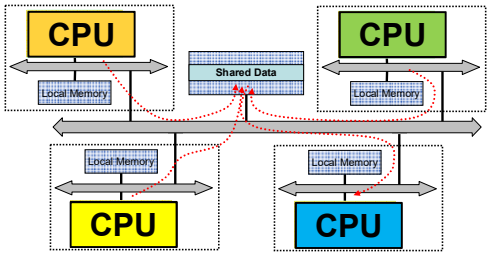
Single core, simple



Multi-core shared memory

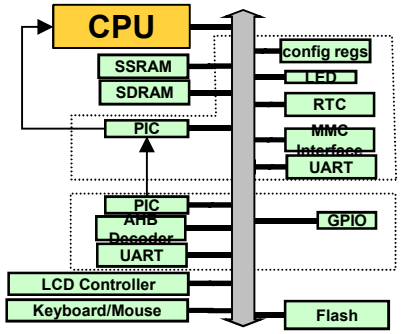


Many-cores

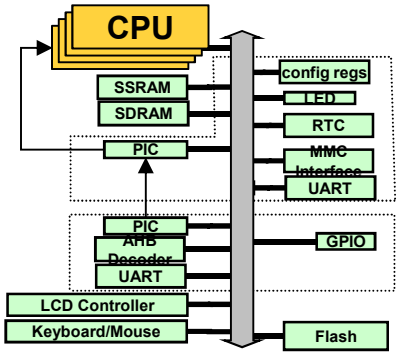


Heterogeneous

Single Core

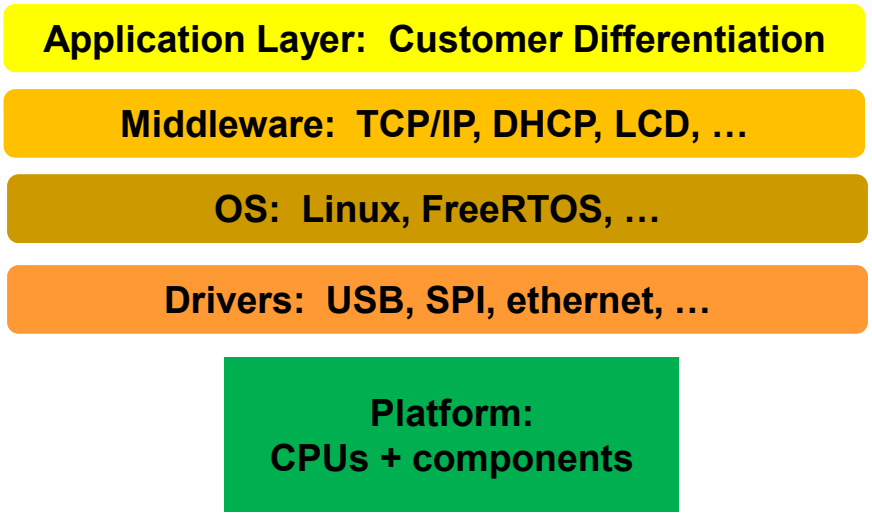


Multi Core (SMP)



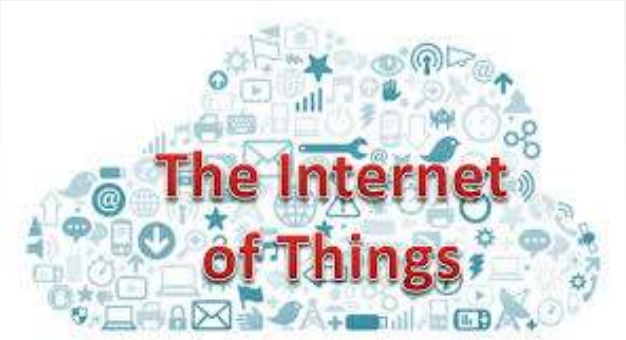
Booting OS, eg Linux

Layers of SW complexity



New Markets With New Software Requirements

- Schedule
- Quality
- Reliability
- Security
- Safety



- Engineering productivity / automation
- Predictability on software development schedules
- Unknown / unmeasurable software delivery risk

Agenda

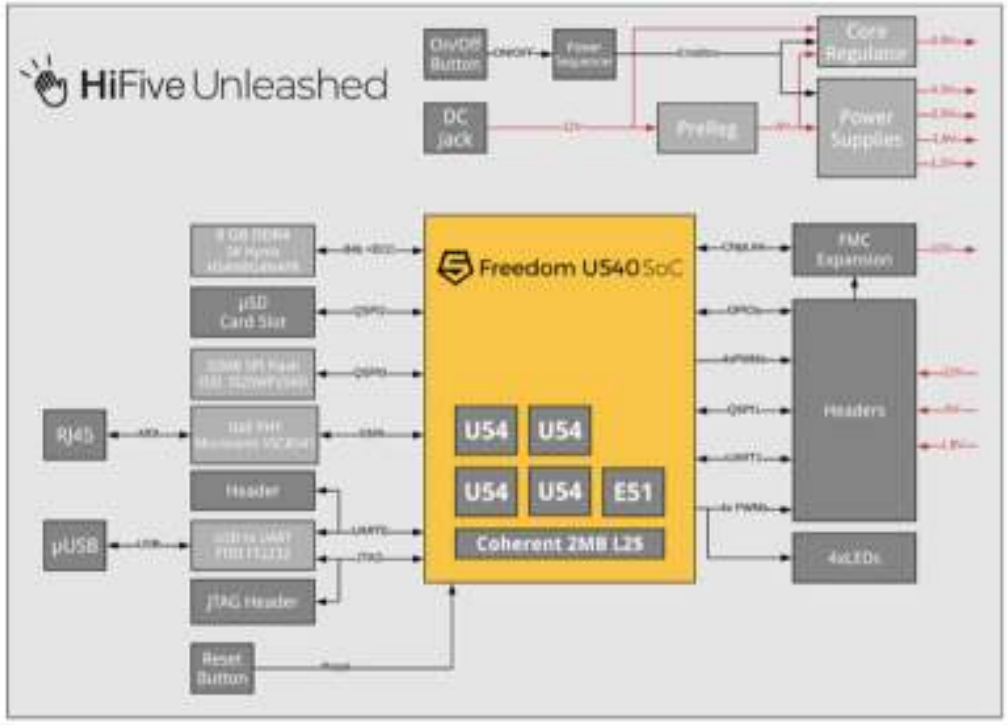
- Introduction to Imperas
- Embedded Software Development Challenges
- Range of Models and Solutions
- Recent News

Virtual Platforms Provide a Simulation Environment Such That the Software Does Not Know That It Is Not Running On Hardware

- The virtual platform is a set of instruction accurate models that reflect the hardware on which the software will execute
  - Could be 1 SoC, multiple SoCs, board, system; no physical limitations
- Run the executables compiled for the target hardware
- Models are typically written in C or SystemC
- Models for individual components – interrupt controller, UART, ethernet, … – are connected just like in the hardware
- Peripheral components can be connected to the real world by using the host workstation resources: keyboard, mouse, screen, ethernet, USB, …
- High performance: 200 – 500 million instructions per second typical, or boots Linux in <10 sec

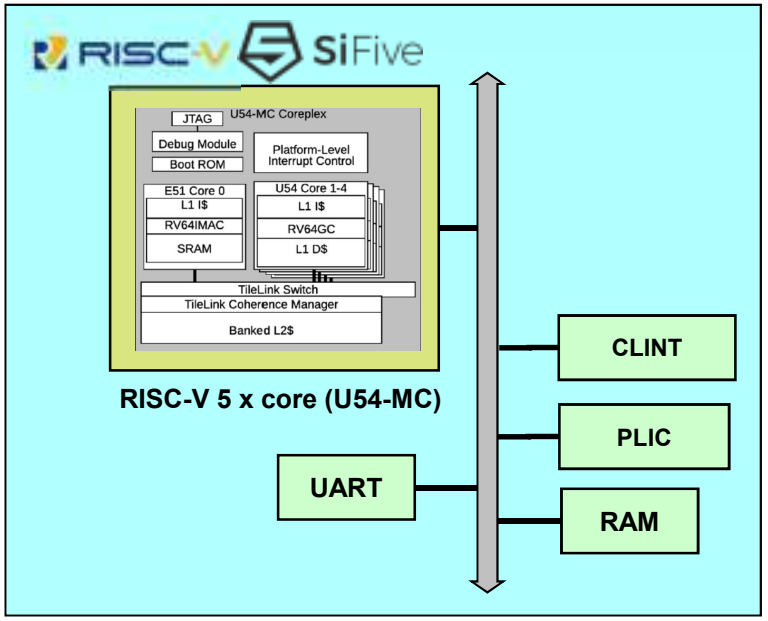
Simulation of RISC-V SiFive U54-MC

The Virtual Platform Provides a Simulation Environment Such That the Software Does Not Know That It Is Not Running On Hardware



https://www.sifive.com

Imperas U54-MC Virtual Platform

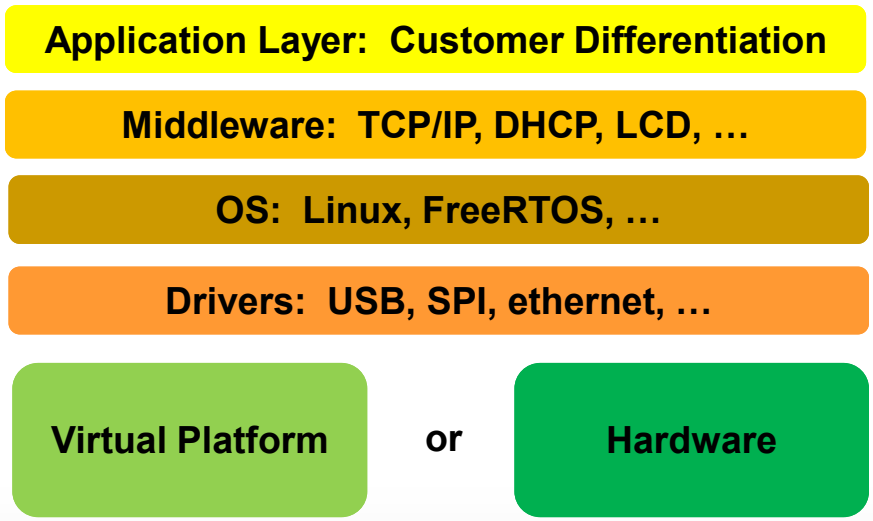


RISC-V 5 x core (U54-MC)

Under 10 seconds to get to booted Linux login prompt!

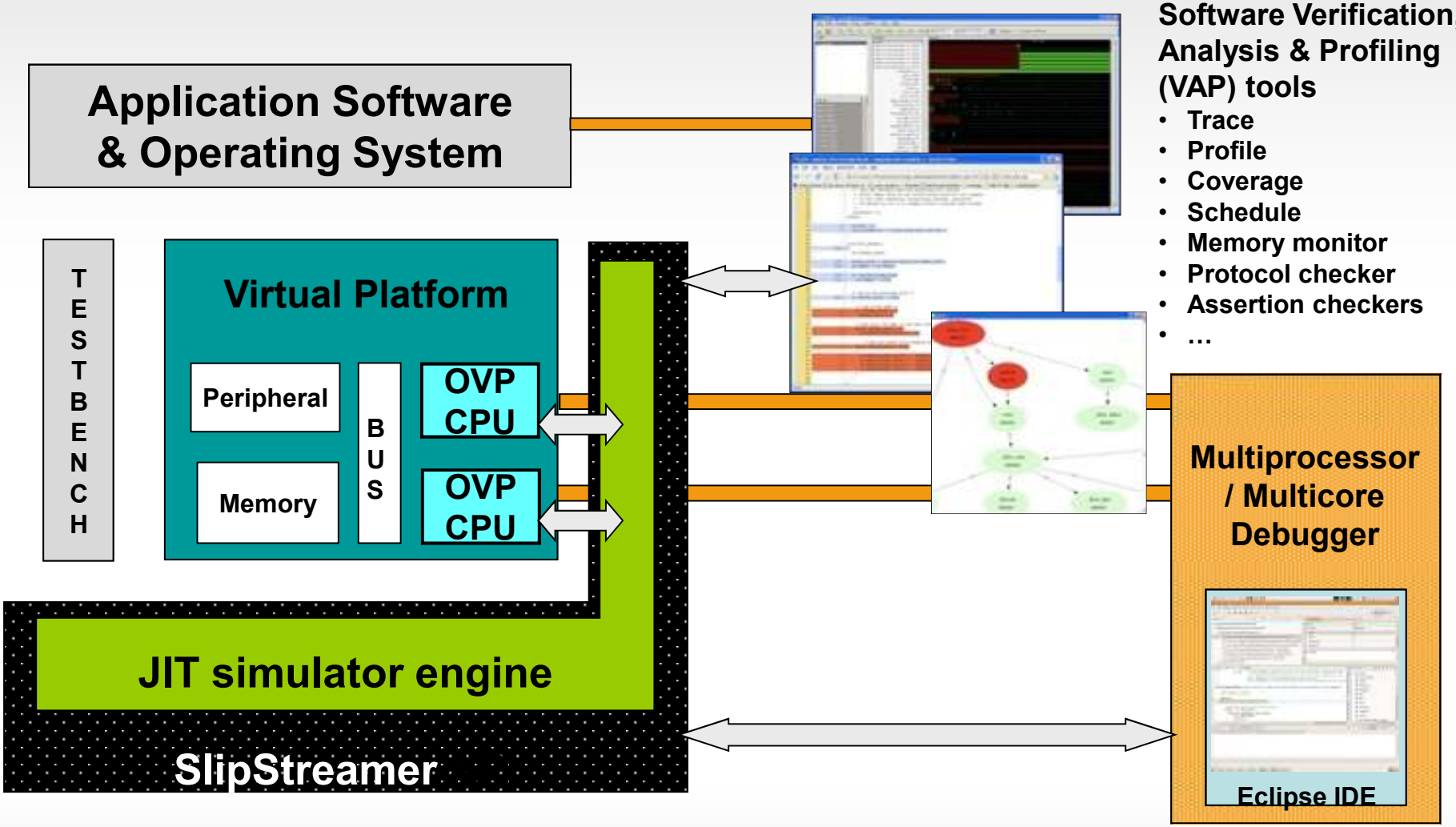
Virtual Platforms are an Integral Part of a Modern Embedded Software Development Methodology

- Virtual platform based methodology delivers controllability, visibility, repeatability, automation, access
  - 75-90% of bugs are functional, and can be found using software simulation testing
- Testing of timing sensitive software, and final testing, still needs to be done on hardware



Virtual platforms – software simulation – provide a complementary technology to hardware platforms

Imperas Tools for Embedded Software Development, Debug & Test



Virtual Platforms Provide a Pre-Silicon Software Development Solution

- Need to start software development earlier in project
  - Before silicon is available
  - Before RTL is available
- Need to port and bring up operating systems
- Need to develop drivers
- Need to develop firmware, test libraries, …

- Because virtual platforms do not require the same level of accuracy as RTL, the virtual platform can be ready months, typically 2-6 months, earlier
- This can mean significant schedule reduction, and/or more time for software testing (higher quality software)

Key Technology: Open Virtual Platforms (OVP) Library of High-Performance Processor Models

- Over 200 Fast Processor Models in OVP Library
- Models and platforms are open source (Apache 2.0 license)
- ARM®: Models for ARMv4™, v5™, v6™, v7™ and v8™ architectures
- MIPS®: Models for nanoMIPS, microMIPS, MIPS32 and MIPS64 architectures
  - Verification, licensing, and distribution relationship
- Renesas: Models for RH850, V850 architectures; 16 bit microcontroller cores
  - RH850G3, V850 ES, E1, E1F, E2; RL78, M16C cores
- Synopsys (ARC): ARC6xx, ARC7xx, EM families
- RISC-V: RV32/64 GCN
  - SiFive E31, E51, U54
  - Andes N25, NX25
- Altera Nios II
- Xilinx Microblaze

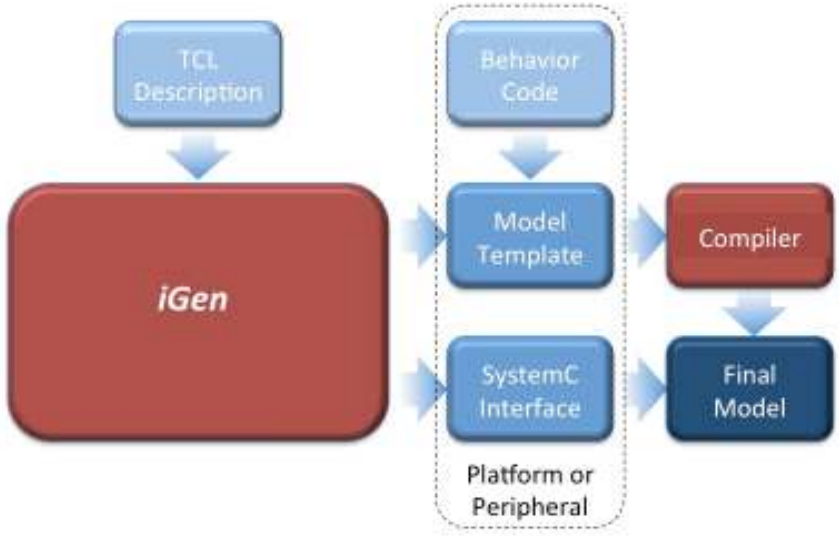
"OVP is addressing key issues in software development for embedded systems. By supporting the creation of virtual platforms, OVP is enabling early software development and helping expand the ARM user community."
Noel Hurley, VP Business Development, ARM

Extendable Platform Kits™ (EPKs™)

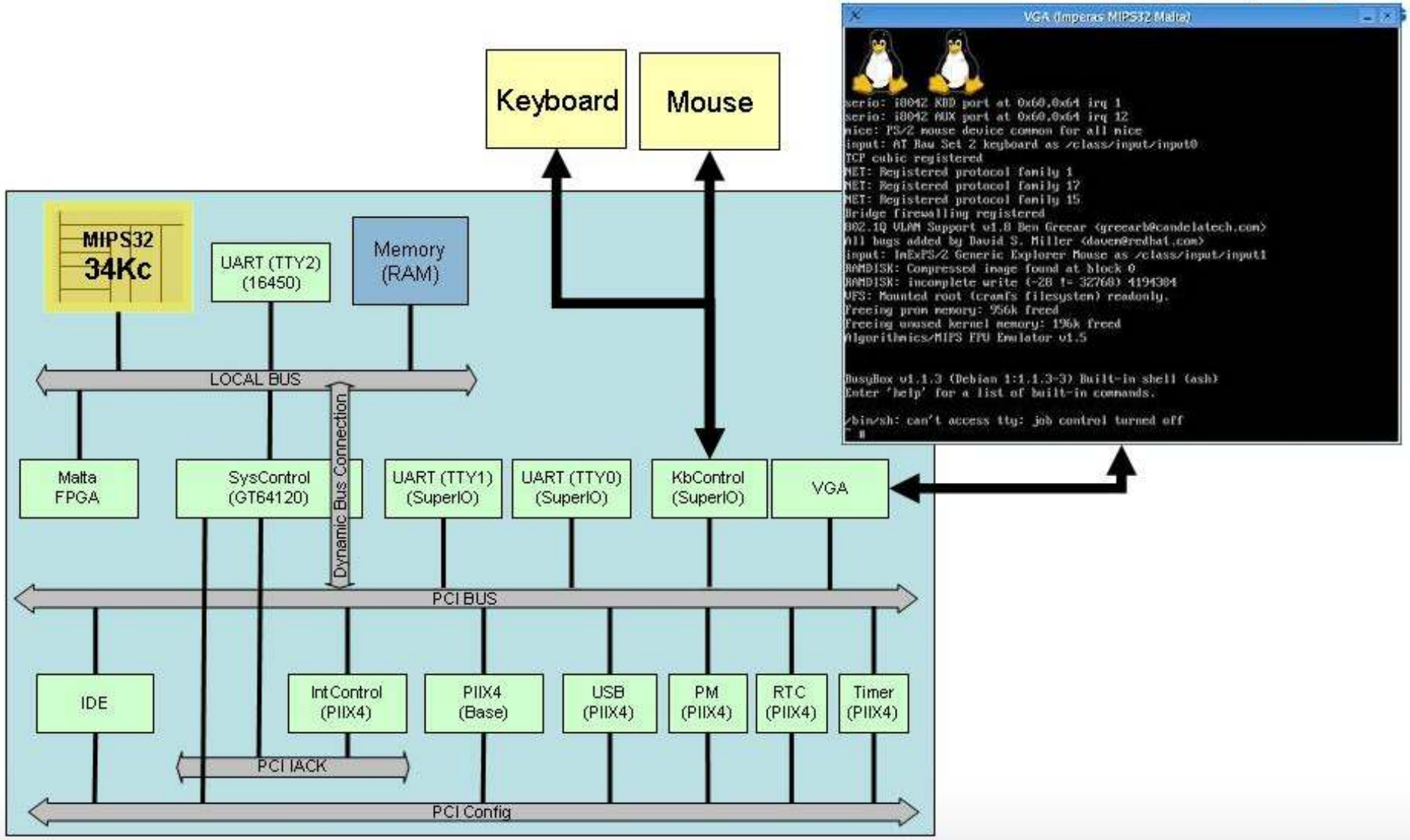
- EPKs are virtual platforms
  - with software set-up, help users to start quickly
- EPKs include
  - Individual models, binary and source
  - Platform model, binary and source
  - Software and/or OS running on platform

- 200+ Processor Models
- 50+ EPKs
- 100s of peripheral models available in the OVP Library
- All models are open source
  - Distributed under the Apache 2.0 open source license
- All models have both C and SystemC interfaces

- Peripherals: users define pins and registers, and functionality
- Platforms: users define memory, component connectivity

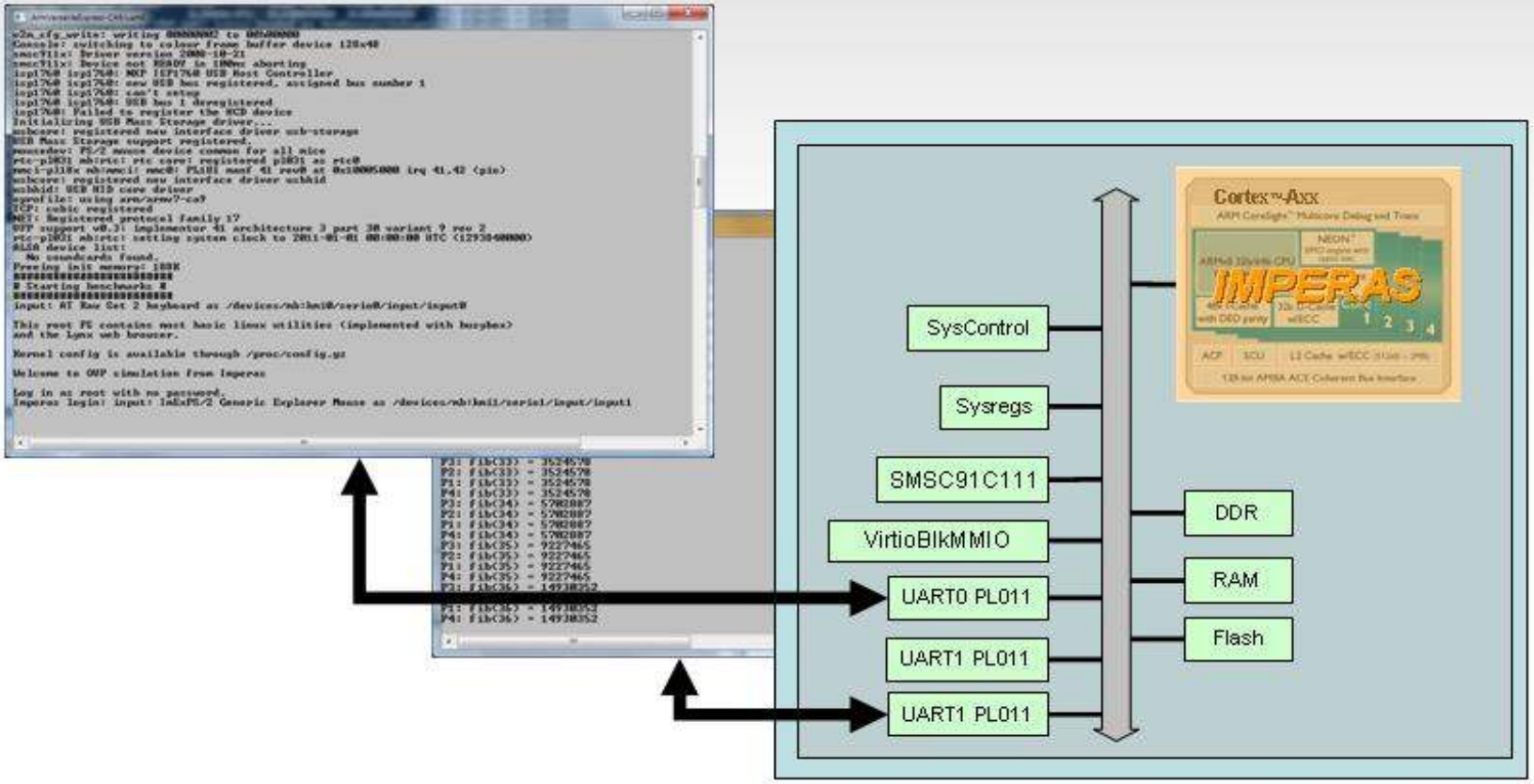


OVPsim MIPS platform
MIPS Malta / MIPS 34K / SMP Linux



Imperas
ARMv8 Linux SMP Kernel

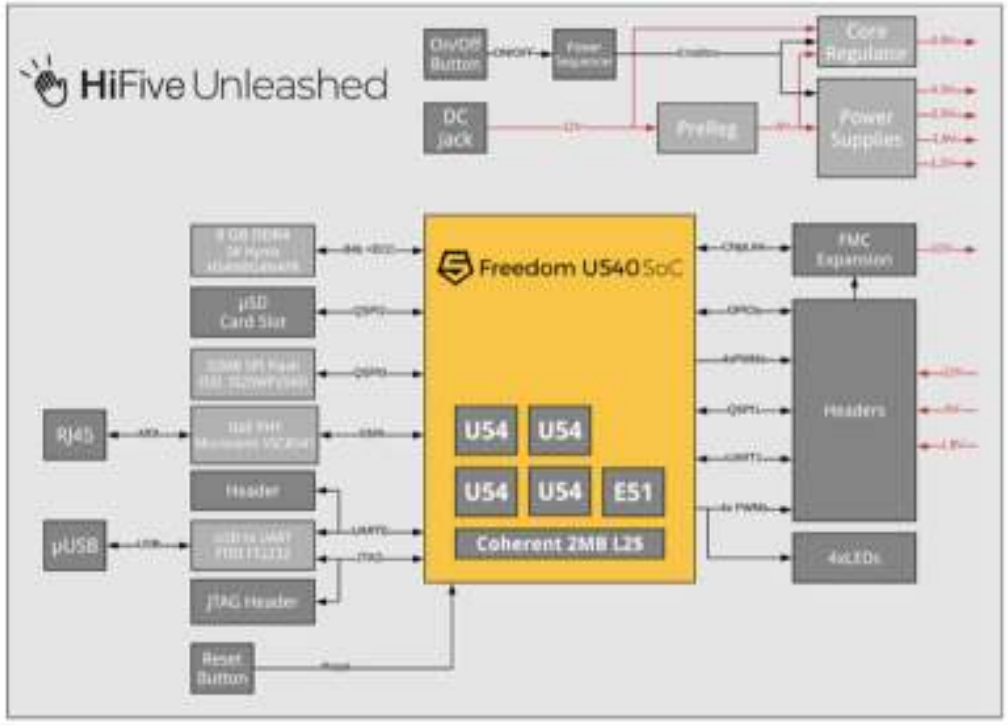
MULTICORE DESIGN SIMPLIFIED
imperas



ARMv8-A-FMv1 Platform

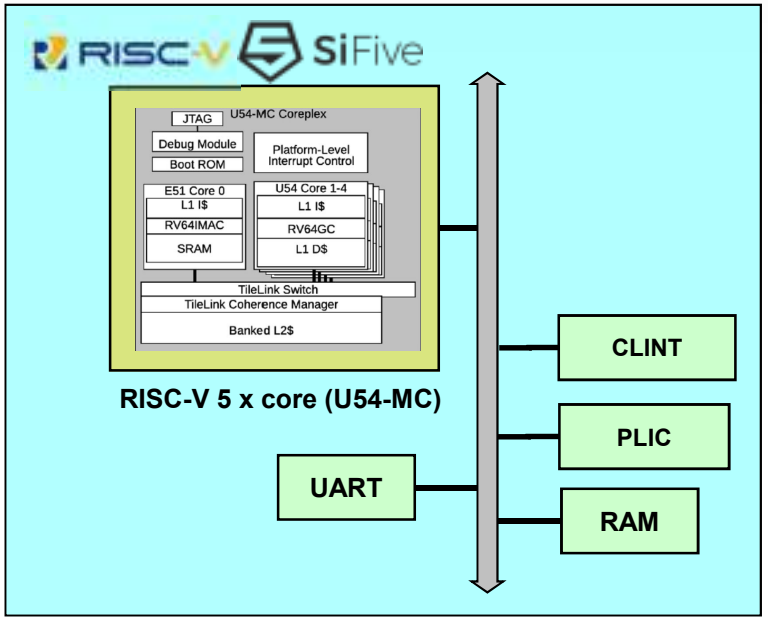
RISC-V EPK based on SiFive U54-MC

The Virtual Platform Provides a Simulation Environment Such That the Software Does Not Know That It Is Not Running On Hardware



https://www.sifive.com

Imperas U54-MC Virtual Platform

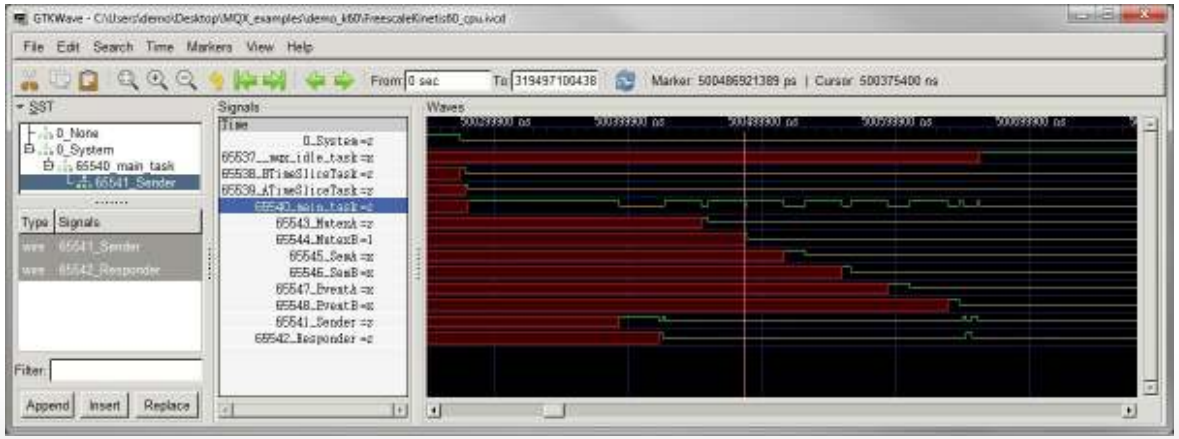


RISC-V 5 x core (U54-MC)

Under 10 seconds to get to booted Linux login prompt!

Advanced Software Tools: OS Aware Analysis

- Application
  - Use virtual platform observability to analyze OS operation (porting, bring up)
- Software test and analysis, with Multi-Core support
  - OS task, event, scheduler non-intrusive tracing
  - Observe process creation, process deletion, context switching,
  - Captures communications between processes
- Imperas M*SDK and OVP Fast Processor Models
  - Support Linux, FreeRTOS, µC/OS, MQX, Nucleus, iTron, …
  - 1-2 weeks to support new RTOS, including proprietary RTOS
  - Now extending tools to support hypervisors



Advanced Software Tools: Code Coverage

- Application
  - Use virtual platform observability to analyze effectiveness of software tests
- Software test and analysis
  - Non-intrusive: no instrumentation or modification of source code
  - Multicore capable
  - Overview and detailed source code analysis reports
  - High performance critical for comprehensive testing

Source Code Detail

Results Overview

"Imperas with its OVP Fast Processor Models is addressing key issues in software development for embedded systems. We are happy to work with Imperas to ensure that high quality models are easily available to our worldwide customers, helping them to develop and test software faster and more easily using virtual platforms."
Hirohiko Ono, senior manager of the MCU Tools Marketing Department, Renesas Electronics

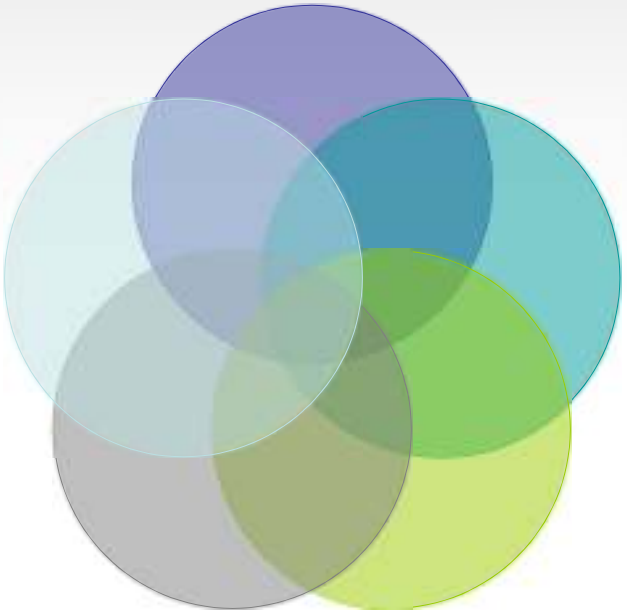
Advanced Software Test Tools: Fault Simulation

- Compliance with standards requires products to demonstrate tolerance to faults
  - Automotive ISO 26262 requires this
- Use Imperas SlipStreamer™ technology to generate, inject, and monitor faults/fault activity
  - Completely non-intrusive; no modification of source
- Use Imperas high speed virtual platform simulation at Instruction Accurate level to analyze software in presence of faults
  - Near real time performance allows complete software stacks and full range of system scenarios to be analyzed

```
FAULT 0x001002a4(   3004905): 0x0000580d -> 0x00005805(^bit= 3) (       mov) 16 Bits
FAULT 0x00100b8c(  12312824): 0x000059e8 -> 0x000059f8(^bit= 4) (       cmp) 16 Bits
FAULT 0x00100b7e(  19676187): 0x00006f0c -> 0x00016f0c(^bit=16) (      ld.b) 32 Bits
FAULT 0x00100b86(  26529726): 0x00006f4c -> 0x20006f4c(^bit=29) (      st.b) 32 Bits
FAULT 0x00100b7a(  34399330): 0x00006007 -> 0x00006087(^bit= 7) (       mov) 16 Bits
```

Imperas Solution Contents

Methodology
Collaboration with customers, vendor ecosystem



Models
200+ CPU models
100's peripheral models
50+ platforms

Tools
Leading simulation, debug, software verification tools

Resources
Imperas and partners
Model development
Tool development

Training
Imperas and partners
On-site, customized agenda

Agenda

- Introduction to Imperas

- Embedded Software Development Challenges
- Range of Models and Solutions

- Recent News

RISC-V Status

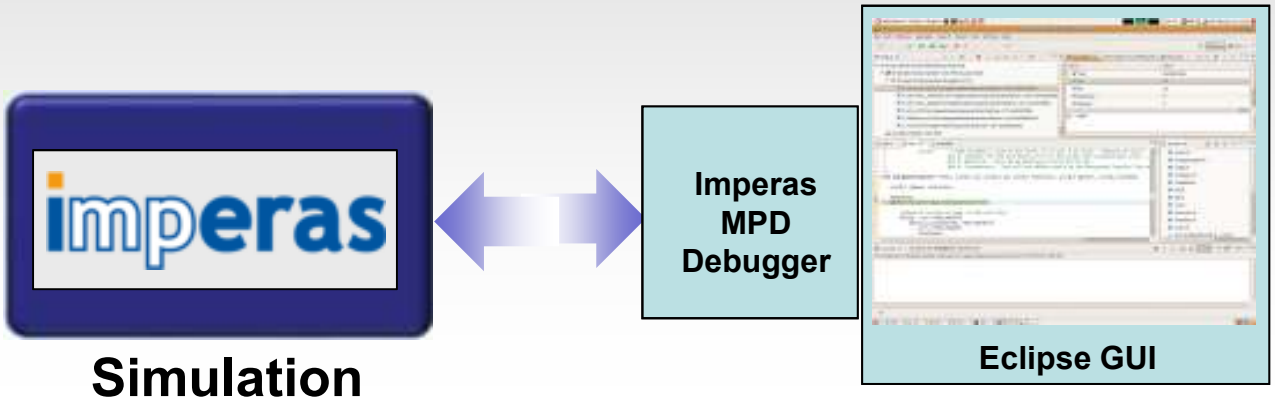
- Processor models
  - RV32/64 GCN, RV32EC
  - Andes N25, NX25 including custom instructions
  - SiFive Mi-V (RV32IMA), E31, E51, U54
  - Added capability to enable easy addition of custom instructions, registers, etc. to processor model via side library
    - Does not perturb known, validated model source
    - All Imperas tools supported for complete model
- Platforms
  - Various RV32 models booting FreeRTOS
  - Single core RV64GC booting Linux in under 5 sec
  - Quad core RV64GCN (SiFive U540 platform) booting SMP Linux in about 7 sec
    - http://www.imperas.com/sifive-risc-v-u54-mc-virtual-platform-booting-smp-linux-being-debugged-with-imperas-multi-core
- Imperas tool support for RISC-V
  - MPD debugger for heterogeneous, multiprocessor/multicore platforms and driver-peripheral co-debug
  - Verification, Analysis and Profiling (VAP) tools including tracing, profiling, code coverage, OS-aware tools, timing estimation (paper at Embedded World)

RISC-V Compliance Work

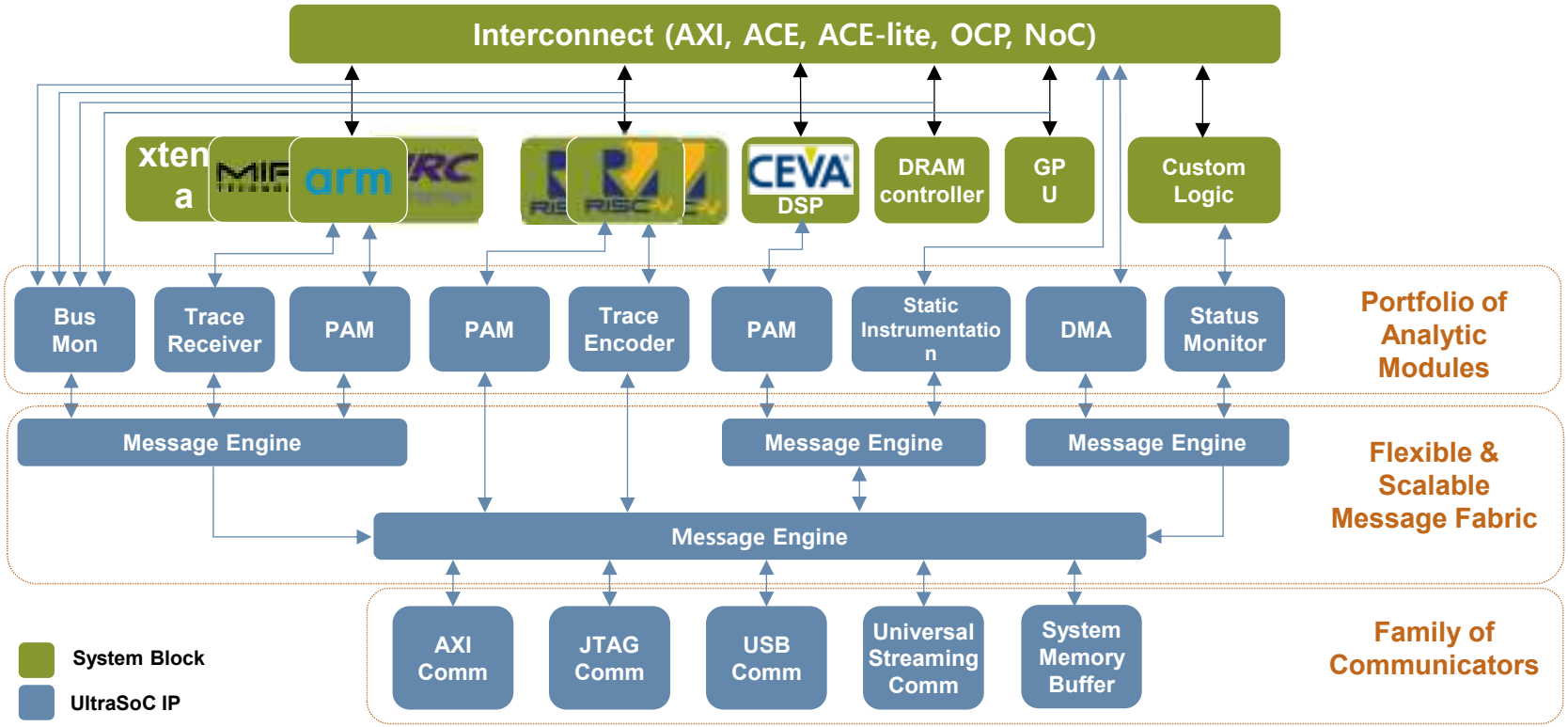
- Active member of RISCV.org Compliance Working Group
  - Driving architecture of test environment
  - Providing infrastructure for better quality compliance tests
  - Working with Formal Model Working Group to develop device configuration file format
- Migrating internally developed tests to be useable in device compliance testing
- Working with customers' RTL developers to check the compliance of their devices to the RISCV.org standards
  - Using Imperas simulation/modeling technology

Collaboration with UltraSoC

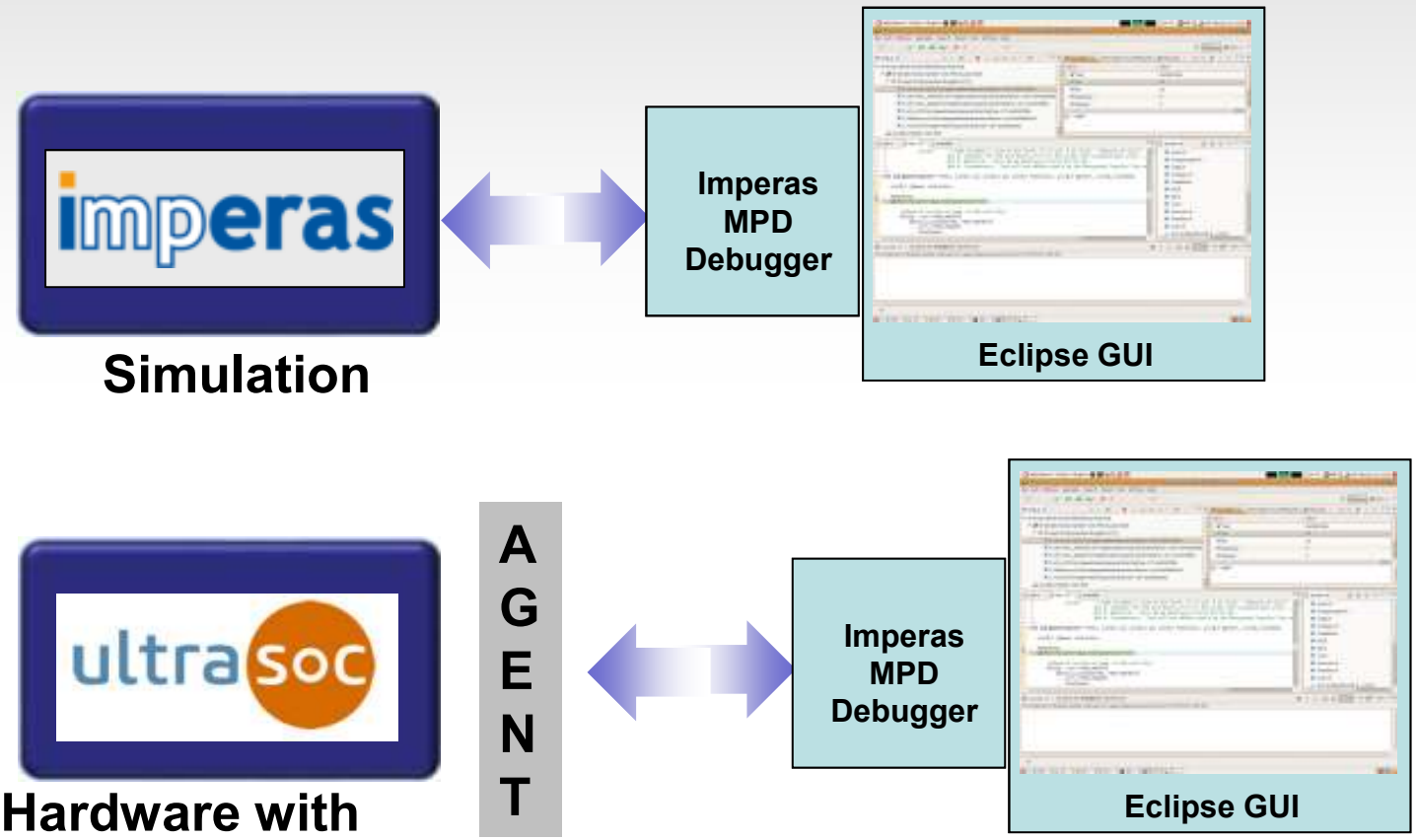
Imperas have full multicore debugger for simulation



Advanced debug/monitoring for the whole SoC



Collaboration



- Common Software Development Environment

Working with Andes

Working with Andes

- Announced in April availability of models of Andes N25 and NX25
  - RISC-V cores with Andes extensions

Working with Andes

- Announced in April availability of models of Andes N25 and NX25
  - RISC-V cores with Andes extensions
- June 2018 – Andes certifies Imperas model as reference


imperas

Revolutionizing Embedded Software Developm

Home Products Solutions OVPworld Resources News

Andes Certifies Imperas Models and Simulator as a Reference for Andes RISC-V Cores

ANDES TECHNOLOGY

Imperas Virtual Platform, Software Simulator and Models for AndesCore N25 and NX25 Processors
Now Certified as a Reference by Andes Technology Corp.

Oxford, United Kingdom, June 21, 2018 — Imperas Software Ltd., the leader in virtual platforms and high-performance software simulation, and Andes Technology Corporation, the prominent CPU IP provider, today announced that Andes has certified the Open Virtual Platforms™ (OVP™) instruction-accurate models and virtual platforms of the AndesCore™ N25 and NX25 IP processors. This rigorous certification program by Andes involves simulation and testing to their highest

Related New

Related Artic

ESL Flow is Dead

Imperas Summary

- Users Benefit From Reduced Schedules & Easy Software Porting and Bring Up
- Key technologies: 200+ processor model library, peripheral model library, fastest simulator, 3Debug, VAP tools
- Strong RISC-V support
- Solutions for internal development and external delivery