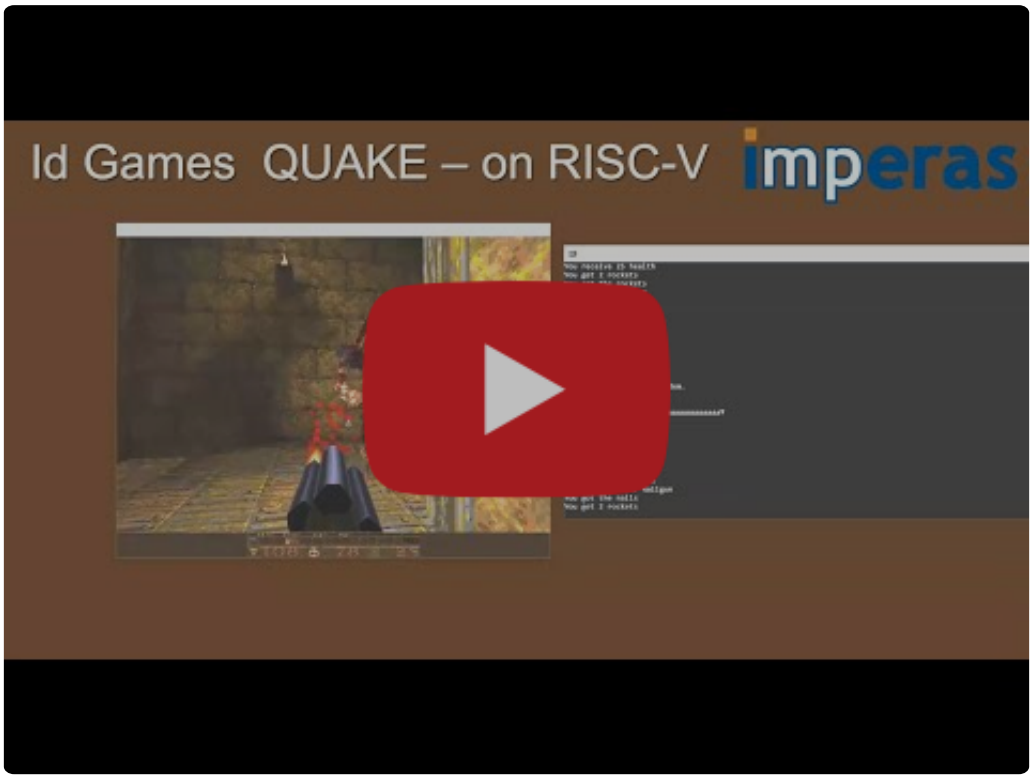
Imperas Newsletter – January 2022

View this email in your browser

imperas

The leader in RISC-V simulation solutions

Software Demo



Watch Quake running on RISC-V with Imperas Virtual Platforms.

This video shows a demo of Quake, originally developed by ID Games, running on an Imperas virtual platform for RISC-V. This demo will also be included within a future update release of OVPsim at: https://www.ovpworld.org

---

Events

RISC-V® Summit

Available On-Demand

DV Keynote talk: Are the RISC-V design freedoms leading to RISK in Verification quality?

The flexibility of RISC-V appears to imply an increase in the design verification scope of work for any SoC project with a customized RISC-V core, this talk introduces the Imperas Reference Model based solutions for RISC-V processor verification.

A video of the talk with **Larry Lapides** is available to watch on YouTube and a PDF of the presentation is available at this link.

Lightning talk: Open-Source RISC-V Cores with Industrial strength verification

This case study explores the background, development and implementation of the **OpenHW** verification environment for CV32E40P, known as **core-v-verif**.

A video of the talk with **Simon Davidmann** and **Lee Moore** is available to watch on YouTube and a PDF of the presentation is available at this link.

Demo Theatre DV talk: Brief introduction to the 5 levels of RISC-V processor verification

This talk reviews the 5 different simulation-based DV flows, ranging from simple signature-based comparisons for architectural validation to advanced 'step-and-compare' flows that support the most complex processors.

A video of the talk with **Kevin McDermott** is available to watch on YouTube and a PDF of the presentation is available at this link.

Demo Theatre SW talk: Software design: porting software to RISC-V using Imperas Virtual Platforms

This talk highlights how simulation and virtual prototypes can be used for software development for new processors and SoCs including a demonstration with Quake running on RISC-V.

A video of the talk with **Katherine (Kat) Hsu** is available to watch on YouTube and a PDF of the presentation is available at this link.

SW Keynote talk: Is hardware/software co-design for applications now a reality with RISC-V?
This talk highlights SoC architectural exploration with multicore arrays and optimized RISC V processors to support early software development for vector accelerators. It introduces some of the challenges and discusses different approaches being adopted in the community/industry.

A video of the talk with **Kevin McDermott** is available to watch on YouTube and a PDF of the presentation is available at this link.

Latest News

Imperas releases new RISC-V verification product that changes the fabric of processor DV
With a combined 100 years of experience and 10 years of effort Imperas creates new ImperasDV killer-app for RISC-V verification engineers.

MIPS selects Imperas Reference Models for RISC-V Processor Verification
Imperas RISC-V golden reference models and Verification IP used for functional RISC-V Processor Verification and Architectural Compatibility Testing.

Codasip Adopts Imperas for RISC-V Processor Verification
Outlines vision for best-in-class RISC-V quality.

Imperas Models – reference for the newly ratified RISC-V Specifications
4Q2021 release of Imperas simulator and reference models supports latest RISC-V Extensions for Bit Manipulation 1.0.0, Cryptographic (Scalar) 1.0.0, and Vector 1.0 plus Privilege Specification 1.12 as RISC-V Board formal approval is completed.

Latest Articles

EDACafé

EDACafé interview with Larry Lapides
Following the announcement of ImperasDV for RISC-V processor verification, EDACafé's **Sanjay Gangal** spoke with **Larry Lapides, VP, Imperas Software**.

To watch the interview, click here.

Following the interview, EDACafé wrote a more in-depth article entitled: **Imperas targets RISC-V verification**, which details how Imperas is addressing the verification challenge of customized RISC-V processors.

To read the full **EDACafé** article by **Roberto Frazzoli**, click here.

Embedded COMPUTING DESIGN

Simplifying Design Verification for Increasingly Custom RISC-V Processors

RISC-V is known as an open-standard instruction set architecture (ISA) whose base instructions have been frozen to minimize complexity. But more recently it has added a wide range of custom extensions and enhancements that are making it increasingly popular amongst SoC designers building application-specific systems.

The custom functionality adopted in these architectures is often enhanced with a hardware/software co-design strategy that optimizes software to maximize the specialized capabilities of the RISC-V processor IP…

To read the full **Embedded Computing Design** article by **Brandon Lewis** & **Saumitra Jagdale**, click here.

ARTICLES FROM SEMICONDUCTOR ENGINEERING
DEEP INSIGHTS FOR THE TECH INDUSTRY

Amdahl Limits On AI

Software and hardware both place limits on how fast an application can run, but finding and eliminating the limitations is becoming more important in this age of multicore heterogeneous processing.

The problem is certainly not new. Gene Amdahl (1922-2015) recognized the issue and published a paper about it in 1967. It provided the theoretical speedup for a defined task that could be expected when additional hardware resources were added, and became known as Amdahl's Law. What it comes down to is that the theoretical speedup is always limited by the part of the task

that cannot benefit from the improvement…

To read the full **Semiconductor Engineering** article by **Brian Bailey**, click here.

Release Information

riscvOVPsim and riscvOVPsimPlus - LATEST NEWS

The latest Imperas and OVP release at the Open Virtual Platforms website.

For an introduction to RISC-V the free single-core envelope model, called **riscvOVPsim**, is an excellent starting point, which can be configured for all the ratified ISA features and includes support of the draft specifications for Bit Manipulation and Vectors.

The latest version was is available via GitHub here.

The free enhanced **riscvOVPsimPlus**, including many more features including full configurable instruction trace, GDB/Eclipse debug, and memory configuration options, plus the RISC-V Vector and other test suites, is now available on the OVP website here.

Has someone forwarded our newsletter to you? Join our mailing list.