RISC-V Models for Verification, Software Development and Architectural Exploration

RISC-V Summit 2022

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13 December 2022

The freedom, and not the free, is why RISC-V usage is growing so fast

High Quality RISC-V Models Are Required for RISC-V Success

- Use cases
  - Architecture analysis, including (especially) custom instructions
  - Software development, debug and test
  - Processor and SoC verification
- Anyone can build an Instruction Set Simulator (ISS)
  - ISS is viewed as a commodity item
  - "Everyone" has built an ISS
- More than an ISS is needed

"For the automotive market our customers expect the highest standards of quality and design assurance. NSITEXE selected the Imperas Vector Extensions Compliance test cases and RISC-V Reference Model as a foundation for our simulation-based design verification (DV) plans."
Hideki Sugimoto, CTO of NSITEXE, Inc., a group company of DENSO Corporation

Imperas and RISC-V

- Imperas founding team has background in Electronic Design Automation (EDA) tools, and FPGA and processor IP companies
- 2007: Imperas founding team saw the need for tools and methodology similar to EDA for software debug, test and analysis, based on software simulation
  - This required high quality models of the embedded processors
  - Self-funded the company, and built a business on virtual platform products serving Arm, MIPS, Renesas, etc. users
- In 2016, we realized the the RISC-V community would need RISC-V models for software development
- While there was, and still is a large demand for RISC-V models for software development, there is also a need for models of custom RISC-V cores, and a need for verification of RISC-V cores
- Imperas started working on RISC-V compliance, and then on processor verification, with RISC-V International and OpenHW Group, and customers such as Nvidia Networking, NSITEXE, MIPS, Codasip, Silicon Labs, and more
  - Imperas developed with riscvOVPsimPlus ISS, and made it freely available, supporting RISC-V processor DV for the complete RISC-V specification
- Now Imperas RISC-V processor models are used in almost every RISC-V project

Imperas RISC-V Customers and Partners

Most RISC-V processor projects use Imperas

Users

- Nvidia Networking (Mellanox)
- NXP
- Silicon Labs
- Seagate
- Nagravision
- Dolphin Design
- lowRISC (Ibex)
- EM Micro US
- Top 10 semiconductor company with embedded, GPU use cases
- Top-tier systems company (AI application)
- Largest automotive ADAS/AI company
- Startup building accelerator based on multiprocessor RV64
- Japanese government projects “TRASIO” and “RVSPF”
- Numerous universities around the world
- 100+ organizations using free riscvOVPsimPlus

Processor IP Partners

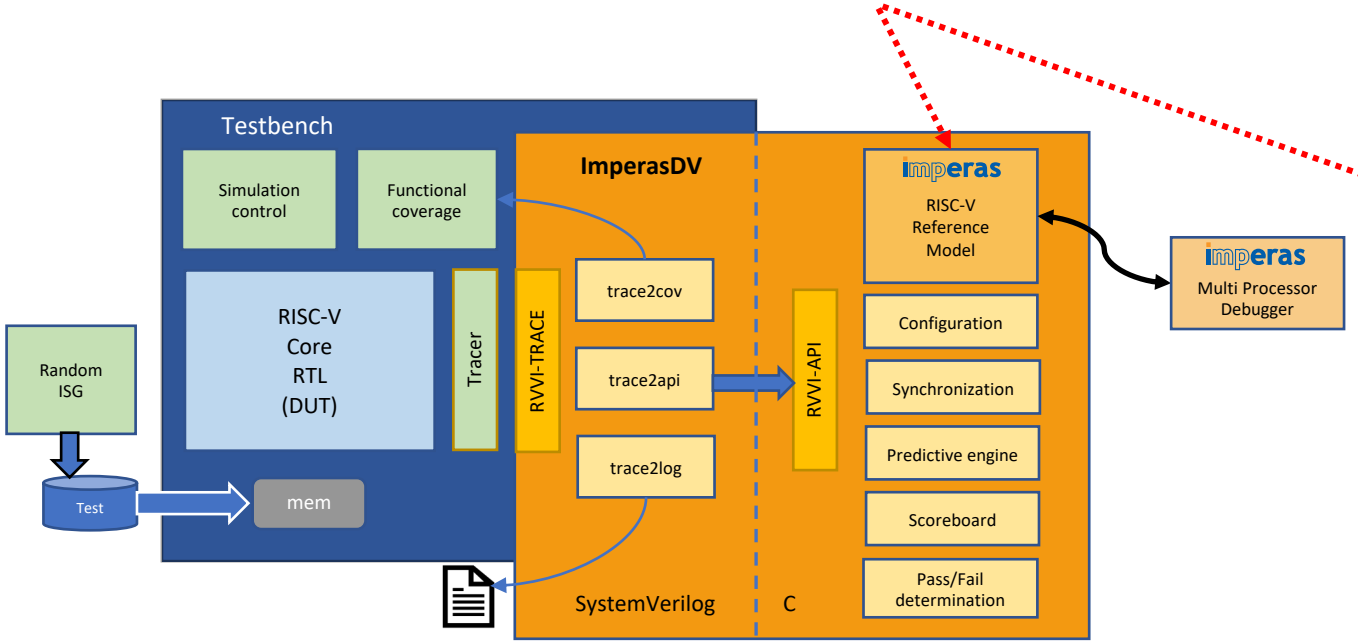
- RISC-V Intl
- Andes (processor IP vendor)
- Codasip (processor IP vendor)
- Intel FPGA (Nios-V processor IP)
- MIPS (processor IP vendor)
- Microchip (Microsemi FPGA Mi-V processor IP)
- NSITEXE (DENSO subsidiary)
- OpenHW Group (Imperas is chair of the verification task group)
- SiFive (processor IP vendor)

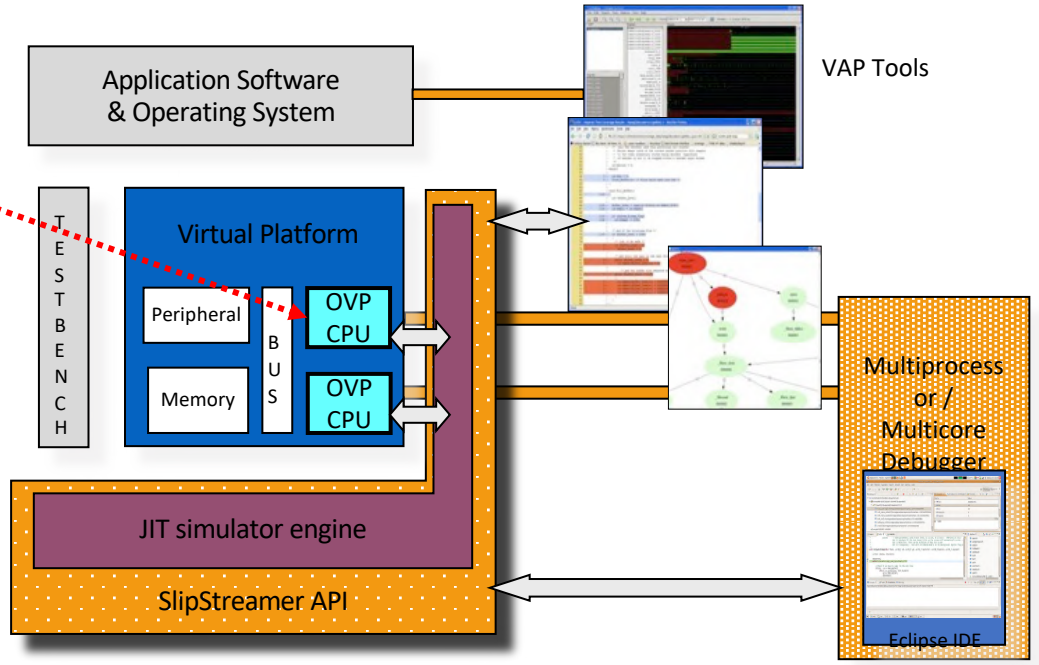
Tool Partners

- Breker
- Cadence (Palladium integration)
- Google (open source ISG)
- Intel (RISC-V Pathfinder IDE)
- Synopsys
- Valtrix (test generation tools)

Imperas OVP RISC-V Models are used for Processor DV & SW Development

- Base model implements RISC-V specification in full
- Fully user configurable to select which ISA extensions/versions
- Imperas provides methodology to easily extend base model





RISC-V Model Requirements

- Model the ISA, including all versions of the ratified spec, and stable unratified extensions
- Model other behavioral components, e.g. interrupt controllers
- Easily update and configure the model(s) for the next project
- User-extendable for custom instructions, registers, …
- Model actual processor IP, e.g. Andes, SiFive, Codasip, MIPS, NSITEXE, OpenHW, Mi-V, …
- Well-defined test process including coverage metrics
- Interface to other simulators, e.g. SystemVerilog, SystemC, Imperas virtual platform simulators
- Interface to software debug tools, e.g. GDB/Eclipse, Imperas MPD
- Interface to software analysis tools including access to processor internal state, etc.
- Interface to architecture exploration tools including extensibility to timing estimation

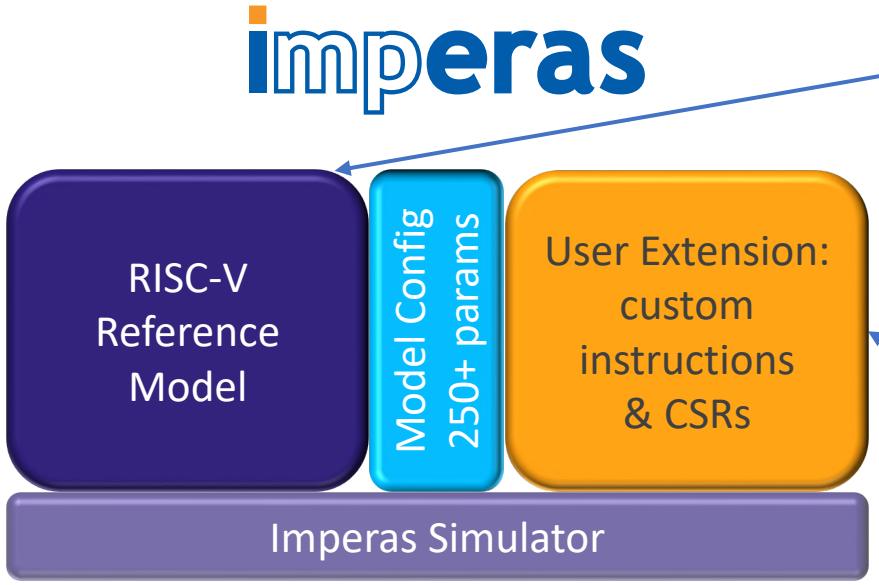
- Most RISC-V ISSs can meet one or two of these requirements
- Imperas models and simulators were built to satisfy these requirements, and matured through usage on non-RISC-V ISAs over the last 12+ years

Open Virtual Platforms (OVP) RISC-V Fast Processor Models

- Use cases
  - Architecture analysis, including (especially) custom instructions
  - Software development, debug and test
  - Processor and SoC verification
- Existing Imperas Open Virtual Platforms (OVP) Fast Processor Models of …
  - Generic or envelope models of RV32/64 IMAFDCEVBHKPZ* M/S/U privilege modes
  - Models of processor IP vendors: Andes, Codasip, MIPS, NSITEXE, OpenHW, SiFive
  - Models for developers building their own processor
- Custom instructions easily added by user or by Imperas
  - New instructions are added in a side file so as not to perturb the verified model
  - Custom instructions are analyzed for effectiveness
- Models are built using Test Driven Development (TDD) methodology
  - Tests are built at the same time as features are added
  - Continuous Integration (CI) test flow used
  - > 15,000 tests for models + simulator
  - Additional testing by processor IP vendors to validate models

"The Imperas virtual platform solutions for software development, debug and test, along with their open-source models, will help accelerate SoC and embedded software development for our customers."
Charlie Hong-Men Su, Ph.D., Andes Technology CTO

Imperas Model Extensibility



- Separate source files and no duplication to ensure easy maintenance
- Imperas or user can develop the extension
- User extension source can be proprietary

Imperas develops and maintains base model

- Base model implements RISC-V specification in full
- Fully user configurable to select which ISA extensions
- Fully user configurable to select which version of each ISA extension
- Fully user configurable for all RISC-V specification options

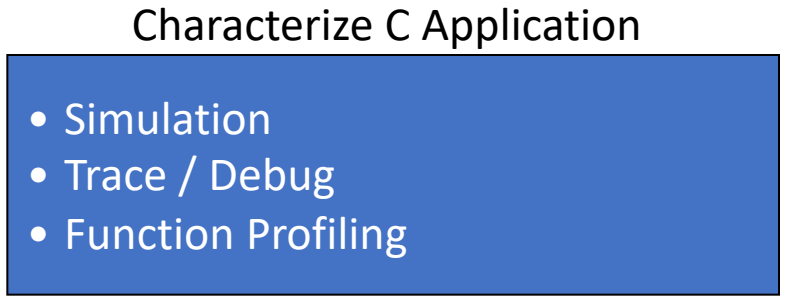
Imperas provides methodology to easily extend base model

- Templates to add new instructions
- Code fragment for adding functionality
- 100+ page user guide/reference manual with many examples

"The donation of a robust, commercial-quality simulator – riscvOVPsim – will enable our customers to adopt RISC-V even faster. This is the level of close industry collaboration that will drive the successful adoption of RISC-V."
Yunsup Lee, co-founder and CTO SiFive

Imperas OVP model is architected for easy extension & maintenance

Flow to Add New Custom Instructions



- Custom instructions are added to optimize a specific application or set of applications within a domain
- Therefore, start by characterizing the application to be optimized
- Then add the custom instructions, evaluate, and iterate

Function Profile C Application

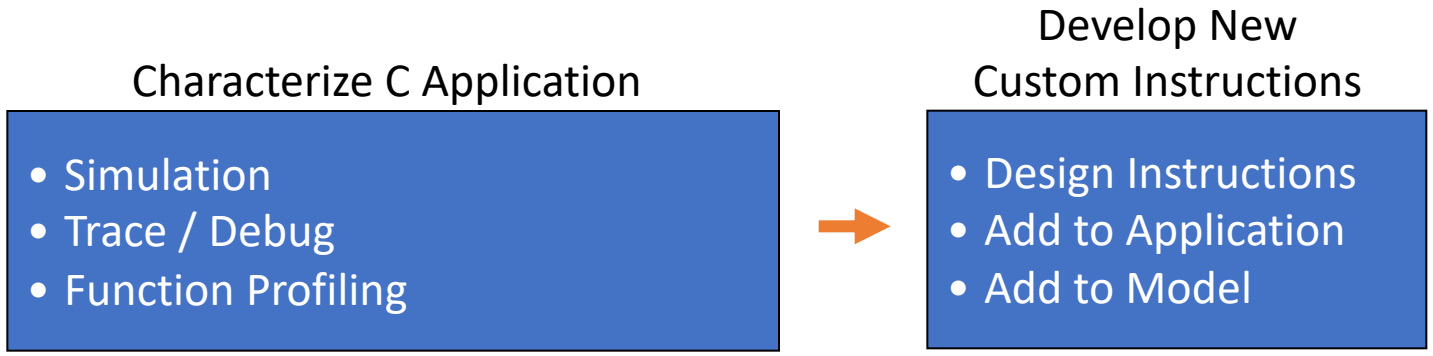
- Same C application
- Sampled profiling with call stack analysis

➢Shows proportion of time spent in each application function

➢21.35% spent in processLine

Name (location)	Arcs in	Samples in	Arcs out	From/To this	Percentage (%)
Platform: iss					
Processor: iss/cpu0					
Process: 0_None		1659204277			
_fread_r	598189652	596534872	1654780		35.95%
processLine	925852930	354236017	571616913		21.35%
qr4_c	150627639	150627639	0		9.08%
qr1_c	146083640	146083640	0		8.8%
qr2_c	137682652	137682652	0		8.3%
qr3_c	137222982	137222982	0		8.27%
__libc_init_array	0	135154865	1524049412		8.15%
__srefill_r	1654780	1024985	629795		0.06%
__sread	629637	321116	308521		0.02%
_read_r	308521	308521	0		0.02%
_fseeko_r	2706	2126	580		0.0%
_vfprintf_r	1874	764	1110		0.0%
__sfvwrite_r	848	752	96		0.0%
rewind	3267	561	2706		0.0%
_close_r	357	357	0		0.0%
_malloc_r	323	297	26		0.0%
__sseek	528	288	240		0.0%
_lseek_r	240	240	0		0.0%
__sfmoreglue	399	224	175		0.0%
_fclose_r	734	204	530		0.0%

Flow to Add New Custom Instructions



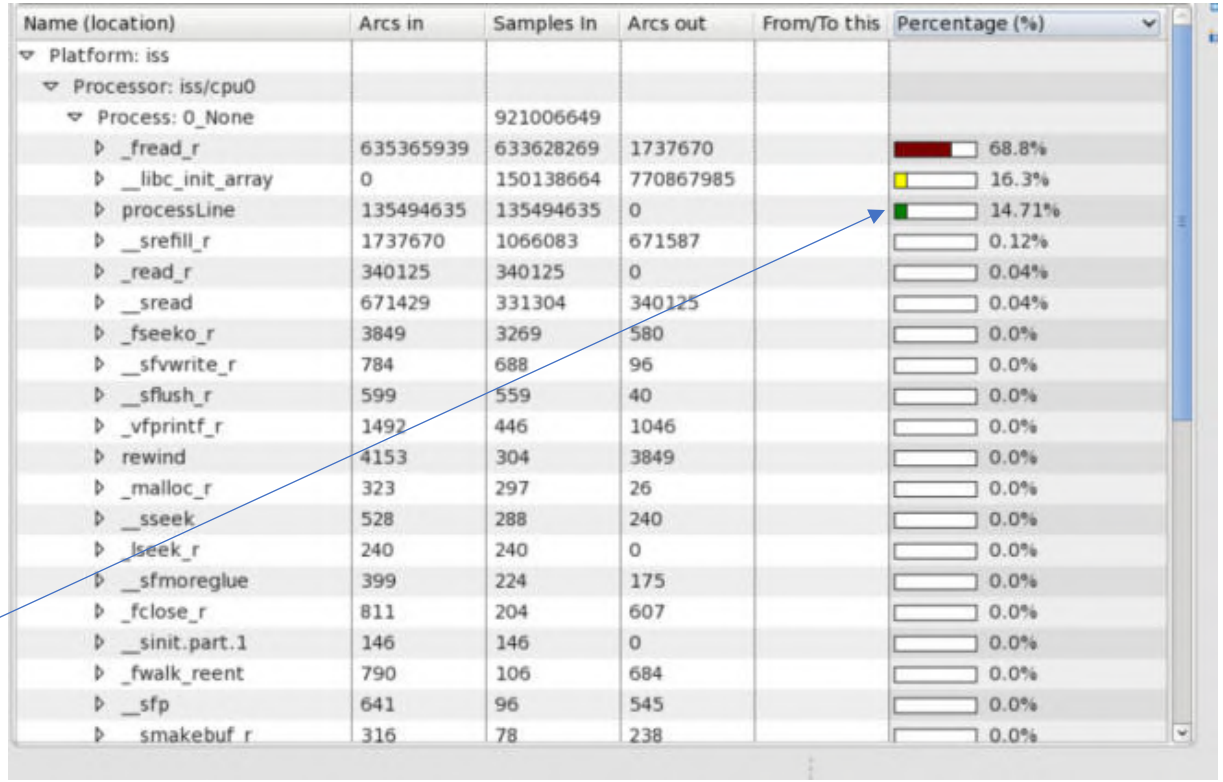
Function Profile Application Using Custom Instructions

- IA simulation + custom instructions with sampled profiling

➢Shows where slowest function is
  - Now much faster…

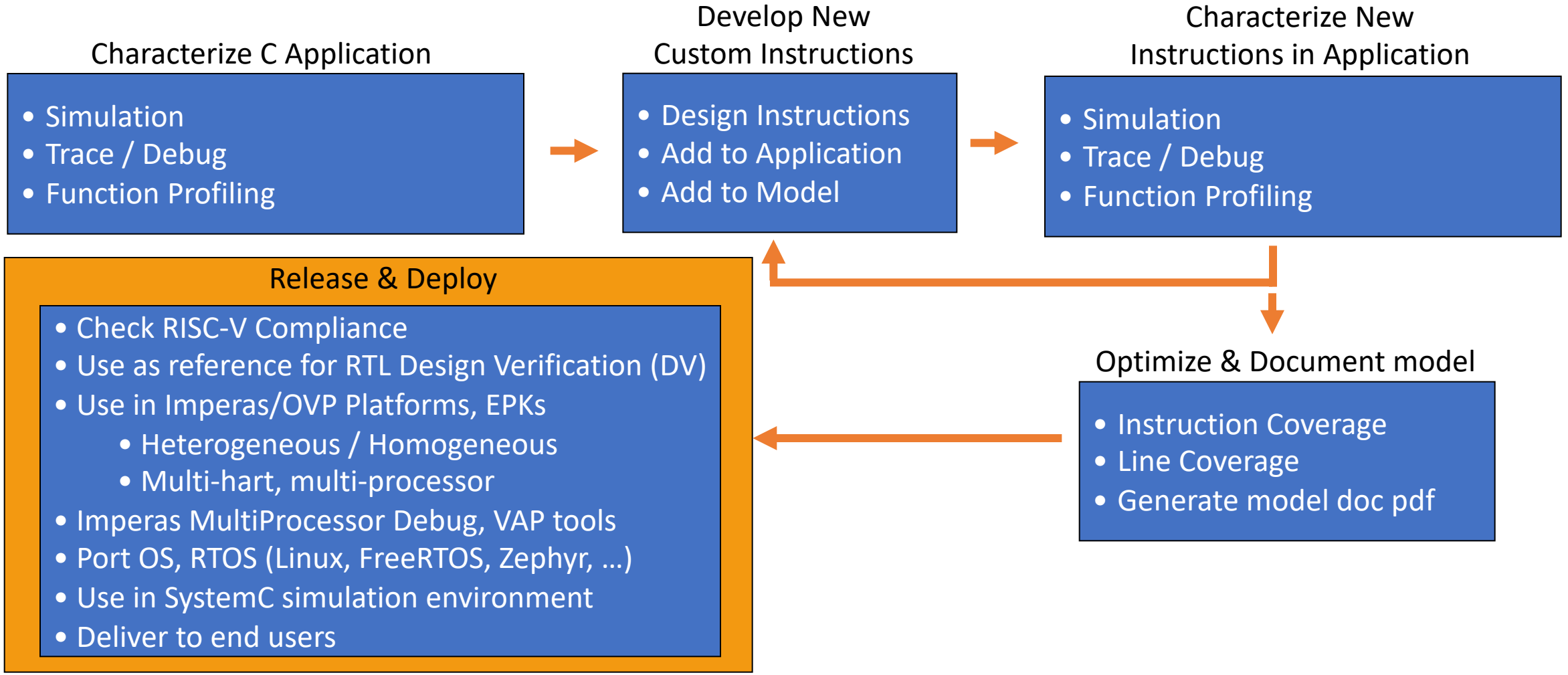
➢Shows benefits of using custom instructions

➢processLine was 21.35% now 14.71%



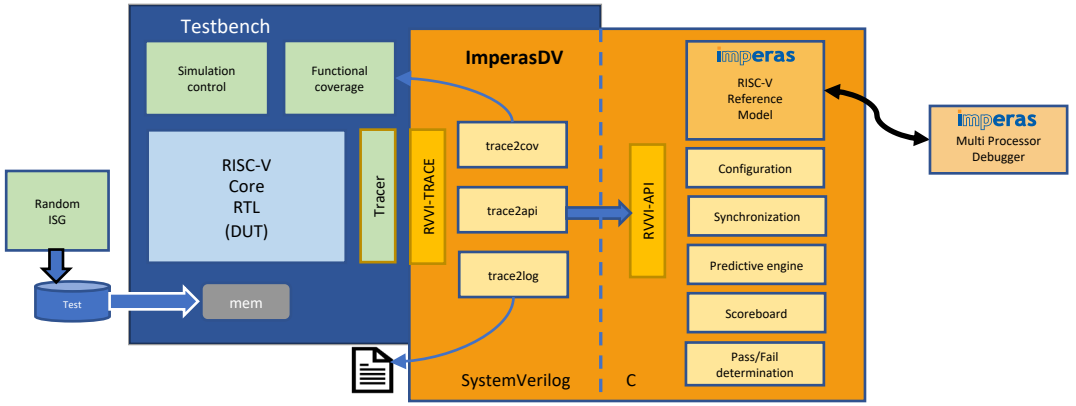
Name (location)	Arcs in	Samples in	Arcs out	From/To this	Percentage (%)
Platform: iss					
Processor: iss/cpu0					
Process: 0_None		921006649			
_fread_r	635365939	633628269	1737670		68.8%
__libc_init_array	0	150138664	770867985		16.3%
processLine	135494635	135494635	0		14.71%
__srefill_r	1737670	1066083	671587		0.12%
_read_r	340125	340125	0		0.04%
__sread	671429	331304	340125		0.04%
_fseeko_r	3849	3269	580		0.0%
__sfvwrite_r	784	688	96		0.0%
__sflush_r	599	559	40		0.0%
_vfprintf_r	1492	446	1046		0.0%
rewind	4153	304	3849		0.0%
_malloc_r	323	297	26		0.0%
__sseek	528	288	240		0.0%
_lseek_r	240	240	0		0.0%
__sfmoreglue	399	224	175		0.0%
_fclose_r	811	204	607		0.0%
__sinit.part.1	146	146	0		0.0%
_fwalk_reent	790	106	684		0.0%
__sfp	641	96	545		0.0%
__smakebuf_r	316	78	238		0.0%

Flow to Add New Custom Instructions



Imperas RISC-V Processor DV Flow: Key Technologies are the RISC-V Reference Models and Verification IP

- Reference model needed for comparison of correct behavior
- Verification IP provides ease of use, saves time and resources
- RVVI standard provides communication between test bench and reference model subsystem
  - https://github.com/riscv-verification/RVVI

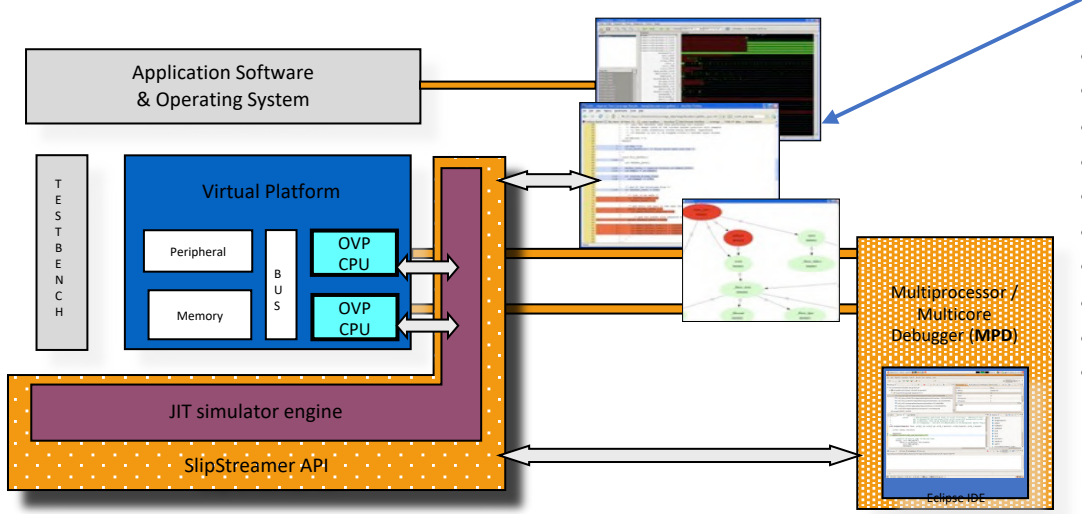


- Feature selection and design choices require serious consideration due to implications of every decision
  - Every addition dramatically compounds verification complexity
  - Adds schedule, resources, quality costs == big risks
- Before 2021, no off-the-shelf toolkit/products available for DV of processors … then came ImperasDV
- ***Imperas reference models + ImperasDV verification IP + RVVI = support for asynchronous-step-compare DV flow***
  - Needed to support features such as interrupts, privilege modes, Debug mode, multi-hart, multi-issue and OoO pipeline, …

Imperas Environment for Software Development, Architecture Analysis

Key technologies/differentiators:

- OVP Fast Processor Models
  - Most models
  - Highest quality
- Simulator engine
  - Highest performance
  - SlipStreamer API for non-intrusive tools
- Tools
  - MPD for platform-centric debug
  - VAP tools for comprehensive software analysis
  - Tools automatically work with custom features in models



Software Verification, Analysis & Profiling (**VAP**) tools

- Trace (instruction, function, variable, …)
- Profile
- Code coverage
- Memory monitor
- Protocol checker
- Assertion checkers
- Fault injection
- OS aware tools
- Timing estimation
- …

- Virtual platforms provide
  - Controllability, observability, determinism, ease of automation, ease of delivery, ease of maintenance
  - Shift left for software schedule, often the critical path to product delivery
  - Performance which enables comprehensive testing of many, many scenarios
- ***Virtual platforms are a must have for software/system of any complexity, or with quality/reliability/safety/security requirements***

Successful RISC-V Projects Need High Quality RISC-V Models

- Karl Benz manufactured the first German car Motorwagen in 1885
- The 2020 F1 car has dedicated team of experts supporting the team to achieve the best potential

- Both cars have an internal combustion engine, and can get you from here to there …
- A RISC-V ISS can get you started
- A real RISC-V model plus simulator is needed for real RISC-V projects
  - For architecture exploration, including custom features
  - For software development, debug and test
  - For processor IP design verification
- Imperas OVP Fast Processor Models satisfy RISC-V project requirements

Thank you

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