Imperas Newsletter – December 2020

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RISC-V Reference Model for Processor DV

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Latest news

RISC-V® Summit

Imperas is a Gold Sponsor at RISC-V Summit

Join us: Keynote panel session, tech talks, tutorial and our virtual booth

Imperas is leading the verification activities at the RISC-V Summit with a keynote panel session on RISC-V verification featuring contributions from commercial and open-source IP providers, an SoC developer plus the verification ecosystem.

For SoC designers adopting RISC-V, the prospects of tackling the processor DV tasks may be a new challenge. The established SoC flows have a couple of standard assumptions – test benches written for UVM SystemVerilog flows and known good processor IP from a mainstream supplier. Now with RISC-V, processor IP cores can be from a variety of sources, including commercial, open source and internally developed. In addition, options to extend or modify a processor make the processor DV task something all adopters will need to consider. Based on working with some popular open-source cores our RISC-V Summit talk and tutorial will feature the experiences of working with flows, test benches and methodologies with SoC DV teams exploring the full flexibility of RISC-V.

AI and Machine Learning are some of the key market segments looking at RISC-V for domain specific solutions. Learn how Imperas virtual platforms help architecture exploration for many core arrays and custom RISC-V instructions.

Imperas at RISC-V Summit

Events

Articles

Design & Reuse

ISA optimizations for hardware and software harmony: Custom instructions and RISC-V extensions

By Kevin McDermott, Imperas Software Ltd

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SEMICONDUCTOR ENGINEERING
DEEP INSIGHTS FOR THE TECH INDUSTRY

Is Hardware-Assisted Verification Avoidable?

Simulation is no longer up to the task of system-level verification, but making the switch to hardware-assisted verification can lead to some surprises if you do not fully plan ahead.

BY
BRIAN BAILEY

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DEEP INSIGHTS FOR THE TECH INDUSTRY

Speeding Up AI With Vector Instructions

Uses, challenges and tradeoffs in working with vector engines.

BY
ANN STEFFORA MUTSCHLER

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Release information

OVP and riscvOVPsim RELEASE NEWS

The latest Imperas and OVP release at the Open Virtual Platforms website.

For an introduction to RISC-V the free single core envelope model, called riscvOVPsim, is an excellent starting point, which can be configured for all the ratified ISA features and includes support of the draft specifications for Bit Manipulation and Vectors.

The latest version was uploaded on 13 November 2020, Version: 20201113.0 and is available via GitHub here.

The free enhanced riscvOVPsim, including the RISC-V Vector test suite, is now available on the OVP website here.

riscvOVPsim, learn more

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