Imperas Newsletter – Dec. 2022

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The leader in RISC-V simulation solutions

Imperas RISC-V Summit Kickoff Party

Join Imperas at the RISC-V Summit Kickoff Party on December 12th. You don't need to be registered for the RISC-V Summit, or be a member of RISC-V to attend the party.

Connect with influencers, developers and users in the RISC-V ecosystem as we celebrate the evolution of RISC-V and our community.

The fun starts at 5:30pm on the Market Terrace, San Jose Convention Center.

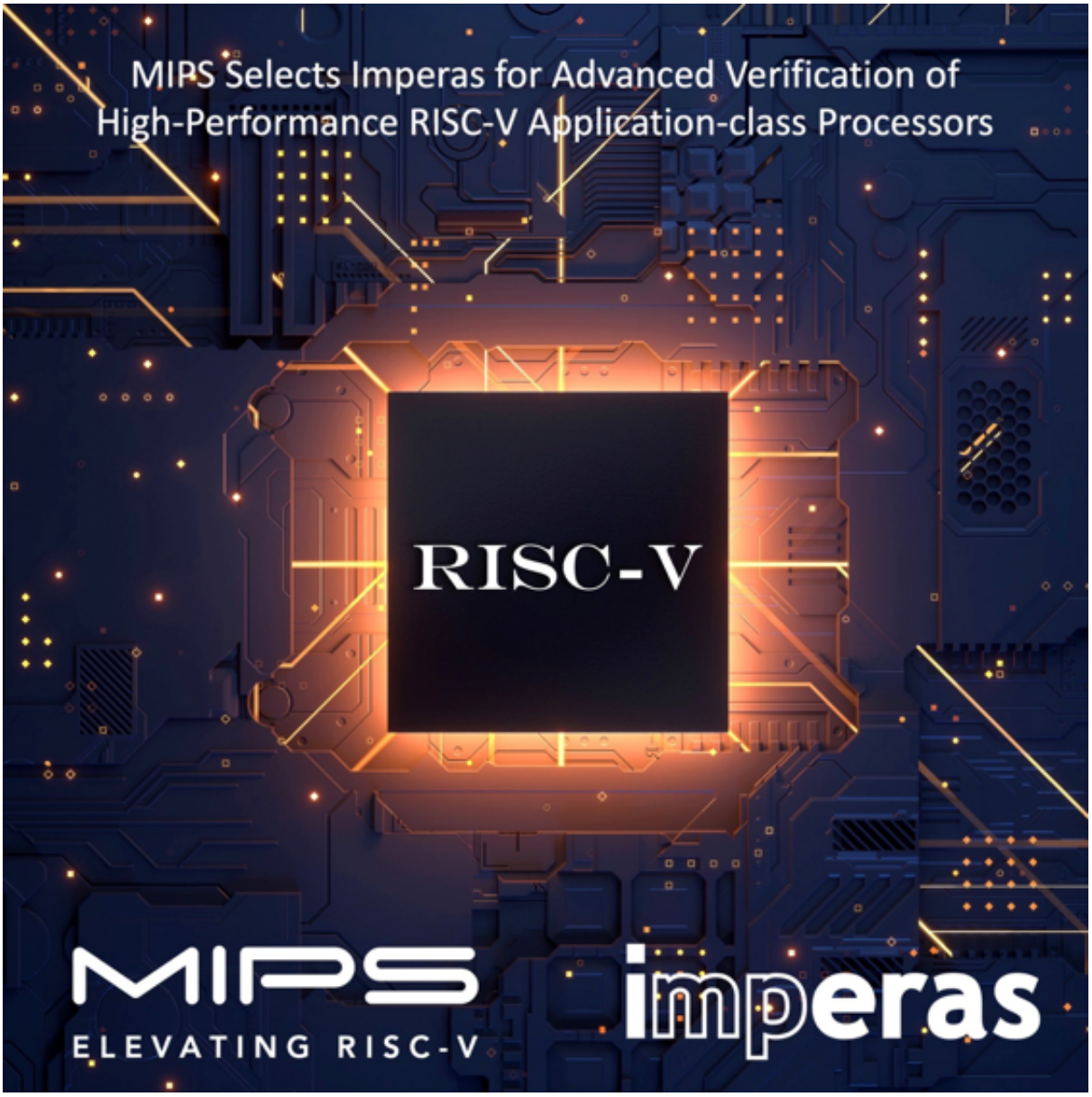
For more information, please click here.

News

“The pace of innovation in markets such as the latest 5G communication networks and infrastructure offers many opportunities for new domain-specific SoC solutions,” said **Chris Porthouse, Chief Product Officer at Imagination Technologies**. “As a leading supplier of silicon IP, we fully appreciate the role

of the ecosystem in supporting our lead customers in delivering new devices to market. We are pleased Imperas have now released the first Catapult RISC-V CPU Imperas reference model for the IMG RTXM-2200, which provides our mutual customers a proven path to accelerate projects to market."

For more information, please click here.



"At MIPS we are experienced in bringing advanced computing technology, such as hardware multi-threading, to market as applications-class processors," said **Don Smith, Vice President Engineering at MIPS**. "As part of the strategic move to RISC-V, we fully appreciate the needs, implications and requirements for a high-quality verification solution. The Imperas Reference Model enables lock-step-compare with asynchronous events, which is the foundation of our SystemVerilog testbench and verification methodology."

For more information, please click here.

“RISC-V represents the potential for innovation, and it is the implementation of great ideas that are really generating exceptional results,” said **Dr. Charlie Su, President and CTO at Andes Technology Corp**. “To unlock such potentials, Andes provides the AndeSysC™ environment, an extensible and near-cycle accurate SystemC model library for all AndesCore®. SoC architects can use it to construct a SystemC based virtual platform for performance evaluation of critical code segment and hardware/software co-optimization. ACE technology helps users implement custom functions and instructions, and it directly connects to the AndeSysC™ environment. Now with the close integration with the Imperas fast reference models and tools, design teams can embark on architecture exploration with complete application software for the next generation of domain specific devices with a seamless path to ACE implementation.”

For more information, please click here.

“Fundamental to the OpenHW CORE-V open-source processor family is high-quality verification that has been achieved with the help and support of the dedicated OpenHW members and contributors,” said **Rick O’Connor, President & CEO OpenHW Group**. “I am excited that Simon is lending his verification expertise and vision to expand the scope of the OpenHW Verification Task Group to address industry-wide standards and methodologies for all RISC-V adopters.”

For more information, please click here.

RISC-V Summit 2022

RISC-V® Summit

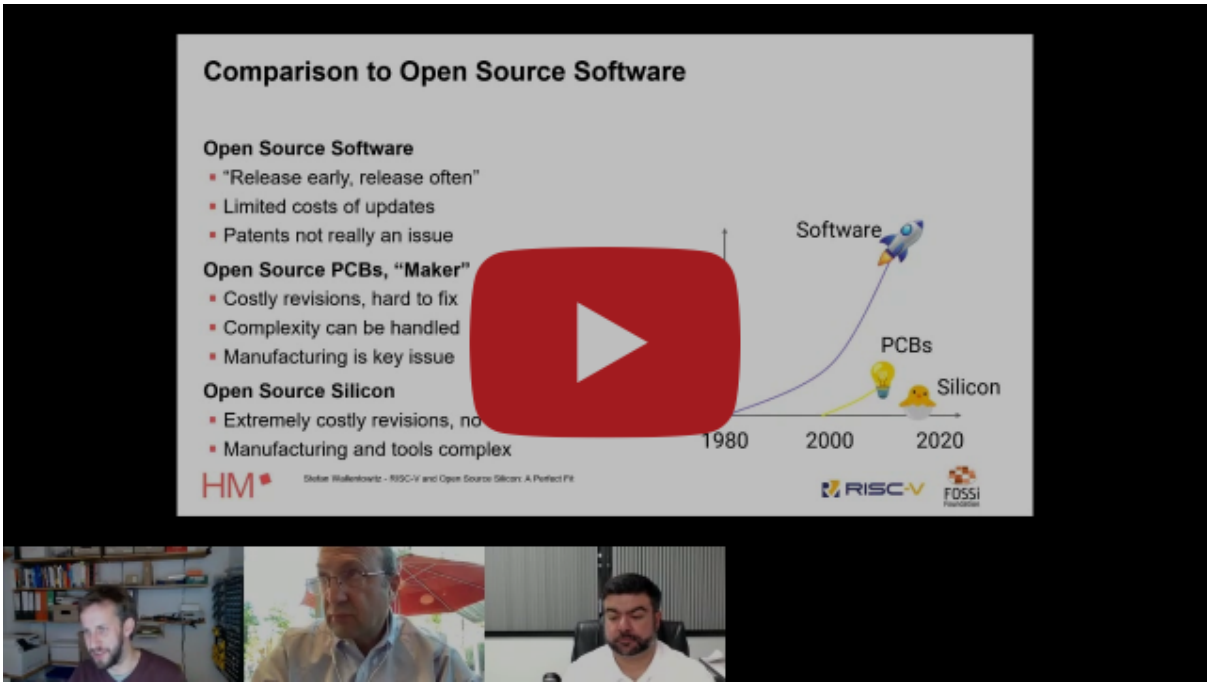
Please stop by the Imperas **booth #D3** and see all the latest demonstrations of simulation and virtual platform technology for RISC-V based designs, including RISC-V processor Design Verification (DV) and architectural exploration with custom instruction, plus support for the latest RISC-V specifications for Vectors and Bit Manipulation. For more information, or to set up meetings with the

Imperas team at the RISC-V Summit 2022, please contact info@imperas.com.

For more information on the Imperas Keynote on RISC-V Processor Verification, plus all the Technical Talks, Exhibit, and Tutorial, see RISC-V Summit 2022.

Videos On-Demand

DVClub on RISC-V Verification Strategies
Simon Davidmann presents RISC-V processor verification with new open standard RVVI based methodology.
Download the slides here.



RISC-V NewYork Group Meeting

Larry Lapides presents The RISC-V Ecosystem: Building In Flexibility With Compatibility.

Articles

ARTICLES FROM SEMICONDUCTOR ENGINEERING
DEEP INSIGHTS FOR THE TECH INDUSTRY

Improving Concurrent Chip Design, Manufacturing, And Test Flows

Realizing the benefits of digital twins is more complicated than translating data between tools...

To read the full **Semiconductor Engineering** article by **Ann Steffora Mutschler**, click here.

The Drive Toward Virtual Prototypes

Prototypes are transforming rapidly to take on myriad tasks, but they are hampered by a lack of abstractions, standards, and interfaces...

To read the full **Semiconductor Engineering** article by **Brian Bailey** click here.

Release Information

riscvOVPsim and riscvOVPsimPlus - LATEST NEWS

The latest Imperas and OVP release at the Open Virtual Platforms website.

For an introduction to RISC-V the free single-core envelope model, called **riscvOVPsim**, is an excellent starting point, which can be configured for all the ratified ISA features and includes support of the latest ratified specifications including Bit Manipulation, Crypto (scalar) and Vectors.

The latest version is available via GitHub here.

The free enhanced **riscvOVPsimPlus**, including many more features including full configurable instruction trace, GDB/Eclipse debug, and memory configuration options, plus the RISC-V Vector and other test suites, is now available on the OVPworld website here.

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