Season's Greetings 2020

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RISC-V Reference Model for Processor DV

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Message from the CEO

A look ahead to next year and 2020 round-up

Happy Holidays! from all of us at Imperas, and thanks for your continued support as we all worked through the most challenging of years. We have achieved a lot and appreciate the help and support across the tech community. While the pandemic has had a huge impact on all of us, I hope you and your family are doing well and best of wishes for the year ahead.

We have seen increasing adoption of our multicore debug and analysis tools

across many applications, including the emerging designs for AI and Machine Learning. These design teams are also using virtual platforms as part of the early project phase for architectural exploration.

We have been supporting the flexibility of RISC-V across an increasing number of projects and have made significant progress in hardware DV (Design Verification) by adapting the SoC verification methodologies to cover the scope of RISC-V processor RTL functional verification. A key breakthrough achievement was highlighted by demonstrating our RISC-V reference model encapsulated in all the mainstream EDA environments for a SystemVerilog UVM step-and-compare flow, a first for RISC-V processor DV.

I would like to take this opportunity to mention many of our supporting customers, users, and partners that have contributed to our success this year:

- The adoption of Imperas RISC-V reference model by Mellanox (NVIDIA), OpenHW, Silicon Labs, NSITEXE, Seagate, and others yet to be made public.
- Our partners such as Arm, MIPS, Andes, Google, Valtrix, Cadence, Mentor, Synopsys, Metrics, and Xilinx, plus other partners and projects we are yet to announce in detail.
- Our distributors: eSOL Trinity (Japan), Coontec (Korea) and QLS (Quantum Leap Sales) for North America.
- Our new users adopting the free riscvOVPsim Reference Model for RISC-V test development and verification with riscvOVPsimPlus using the new free test suites.

I would also like to welcome the latest staff member to the Imperas team, Katherine (Kat) Hsu, who joins us with experience in embedded software and simulation/modeling from Virtutech, QNX, WindRiver, and HPE, and most recently was involved with RISC-V at Hex Five. Kat, who is based in Silicon Valley, will be joining Larry and Manny to support our customers.

For 2021 we plan to extend our solutions for RISC-V Processor RTL verification and the reference models for early software development with virtual platforms.

We look forward to continuing to work with you! Please follow Imperas on LinkedIn, Twitter @ImperasSoftware and YouTube.

Simon Davidmann
CEO
Imperas