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Imperas Collaborates with Mentor on RISC-V Core RTL Coverage Driven Design Verification Analysis

Leading commercial simulation technology from Imperas combined with Mentor's Questa SystemVerilog RTL verification platform extends the hardware design verification of RISC-V cores with industrial quality coverage methodologies

We have announced a collaboration with Mentor, a Siemens business, on the latest hardware Design Verification (DV) Flow for RISC-V processor implementations, to ensure an easy to use reference methodology is available to processor developers, users and adopters across the RISC-V ecosystem.

RISC-V as an open ISA (Instruction Set Architecture) that allows many approaches to implement a processor core and provides SoC developers with a wide range of sourcing options, including commercial IP suppliers, open-source projects and self-developed in-house cores. In addition, the Open ISA aspect of RISC-V also permits the SoC developer to extend the standard core configurations with optimized custom instructions or extensions. Coupled with this design freedom is the challenge faced by DV engineers on the verification and test plans required for the next generation of domain-specific devices.

Working with the Google Cloud Open-Source RISC-V Instruction Stream Generator (https://github.com/google/riscv-dv), the team at Imperas, with assistance from Mentor, developed and enhanced the verification flow to compare the same corner case scenario for the functional behaviour of the RTL-under-test, using the Questa™ platform environment against the golden reference model developed by Imperas. This reference model, riscvOVPsim, is available for free on GitHub for both academic and commercial users. The latest development has been to expand the coverage analysis features to assist the DV engineers as they develop comprehensive test and verification plans for a new core implementation, custom extension, or initial assessment of a core prior to SoC integration.

"RISC-V offers processor designers and SoC developers flexibility in design configuration and optimization for the next generation of domain specific devices," said Neil Hand, director of marketing, Design Verification Technology Division at Mentor, a Siemens business. "Our collaboration with Imperas and the golden reference simulator coupled with the Google Cloud Open-Source RISC-V ISG can provide DV engineers with a flow that now includes the critical coverage analysis required to support the latest verification methodologies."

"Verification, or more accurately, the professional DV engineering community, has become one of the critical aspects of all successful SoC designs and first-time tape-out success," said Simon Davidmann, president and CEO of Imperas. "Quality is not an afterthought to a program schedule; verification plans are fundamental and addressing the complexities of the latest designs requires coverage analysis that provides the essential quantitative assessment of quality."

The reference simulator, riscvOVPsim, is free, and available now for download on GitHub https://www.github.com/riscv/riscv-ovpsim, along with the latest RISC-V compliance test suite and framework, also available on GitHub: https://www.github.com/riscv/riscv-compliance. It includes a free to use license from Imperas, which supports commercial as well as academic use. The open-source model is licensed under the Apache 2.0 license.

The riscvOVPsim solution is an entry ramp for development, as well as a compliance testing tool. For developers of more advanced RISC-V designs, who need multi-core support and advanced debug tools, Imperas also offers full-capability virtual platforms of leading RISC-V platforms including the multi-core SiFive U540 and many others. Using Imperas, developers can configure/customize these extendable platforms or develop their own platforms. Further details are available at www.imperas.com/riscv.

Imperas will demonstrate this RISC-V verification flow, at the upcoming DVCon 2020 in San Jose, California, March 2-5, see more details at this link.

Imperas to demonstrate solutions for RISC-V processor verification and extensions with custom instructions at Embedded World, Nuremberg 2020

We will be co-sponsoring the RISC-V Foundation stand at the Embedded World Exhibition and Conference in Nuremberg, 25-27 February 2020.

Hall 3A, stand 536.

We'll be discussing all the latest demonstrations and virtual platform technology for RISC-V based designs, including verification and custom instruction as well as support for the latest RISC-V specifications for Vectors and Bit Manipulation.

In addition to exhibiting on the booth, we will also present two technical papers:

- Impact of RISC-V adaptability on SoC verification methods – by Lee Moore, Lead Engineer at Imperas

Tuesday 25 February, track session #10.3 @15:00
The verification challenges for RISC-V processors and SoCs will be presented. Specific verification flows including new test and instruction stream generators, reference models and metrics will be presented in detail, including the results of using these flows on real processor IP and SoCs.

- Virtual platform-based development environments for low power, mixed level safety-critical systems – by Larry Lapide, VP Sales at Imperas

Wednesday 26 February, track session #4.3.1 @15:00

Discussing the virtual platform methodology employed by SAFEPOWER. Unique tools developed to provide observability into the hypervisor-based system are described, as well as the methods for providing timing and power estimation with sufficient accuracy.

For more information or to meet with us to discuss how to verify the RISC-V cores in your next design at Embedded World please get in touch here.