Imperas Newsletter – February 2022

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The leader in RISC-V simulation solutions

Lead Article

EDACafé

Imperas targets RISC-V verification

"The greatest migration in verification responsibility in the history of EDA," from the few processor IP vendors to the many SoC designers: this, according to **Simon Davidmann at Imperas Software**, is the challenge facing SoC development teams as they take advantage of RISC-V customization capabilities.

In addressing this challenge, Imperas Software has recently launched **ImperasDV**, an integrated solution for RISC-V processor verification, and this in-depth interview with **Larry Lapides** highlights the technology background and the key role of Imperas in RISC-V processor hardware verification…

To read the full **EDACafé** article by **Roberto Frazzoli**, click here.

Events

Imperas will be at DVCon 2022, providing an in-depth tutorial on the latest simulation-based RISC-V processor verification techniques, presentations and a virtual booth with the opportunity to chat 1-1 with the Imperas team.

Introduction to the 5 levels of RISC-V Processor Verification
Co-author: Simon Davidmann, Imperas Software
Co-author: Lee Moore, Imperas Software
When: Monday, February 28th at 9:00-11:00am PST
This tutorial covers some of the options and latest trends in simulation-based RISC-V processor verification based on industry standards with UVM and SystemVerilog test benches. This tutorial includes an in-depth review of the new open standard RVVI (RISC-V Verification Interface), plus examples based on some popular open-source cores, and a comparison of the different DV methods and options.

Introduction to RISC-V CPU design verification
Speaker: Kevin McDermott, Imperas Software
When: Tuesday, March 1st at 12:30-1:00pm PST
With all the design flexibility and innovations supported by the open standard ISA of RISC-V, quality processor verification is now another flexible option.

Imperas RISC-V Design Verification solutions
Speaker: Larry Lapides, Imperas Software
When: Tuesday, March 1st at 1:00-1:30pm PST
With a history based on EDA tools and background of SystemVerilog, the Imperas technology is now at the forefront of RISC-V processor verification.

Visit the Imperas virtual booth and see all the latest demonstrations and virtual

platform technology for RISC-V Verification including custom instructions and support for the latest RISC-V specifications for Vectors and Bit Manipulation.

For more information, or to set up a live 1-1 demo with the Imperas team during the virtual conference, please contact info@imperas.com.

For more information on DVCon 2022, click here.

Introduction to RISC-V processor verification methodology with dynamic testbench for asynchronous events
Speaker: Larry Lapides, Imperas Software
When: February 22, 2022 – 5:00pm (Tel Aviv, Israel)
For SoC designers adopting RISC-V, tackling the processor DV tasks presents some new challenges. The basic RISC-V compliance suite is insufficient to achieve the coverage requirements for a complete DV test plan, and comparison-based testing with predicted results has built-in limitations. This talk will present the latest results from extensively testing some popular open-source cores, including a discussion of a new open standard for test bench interfaces.

For more information on the SemIsrael Tech Webinar, see this link.

Latest Articles

OpenHW Industrial-Grade Verification for Open-Source CORE-V IP Cores
This article gives an overview of the open methodology and standards-based environment for the verification of the RISC-V based open-source CV32E40P core.

To read the full article published by the **OpenHW Group**, click here.

Growth And Enthusiasm At The RISC-V Summit 2021

We [*Codasip*] weren't sure what to expect from our first major attendance at a #RISCVSummit. Although we were a founding member of RISC-V – as we've been saying quite a lot recently – we have been hiding our light under a bushel…

To read the full article by **Rupert Baines**, published by **Semiconductor Engineering**, click here.

ARTICLES FROM SEMICONDUCTOR ENGINEERING
DEEP INSIGHTS FOR THE TECH INDUSTRY

Growth Spurred By Negatives

Unexpected upside driving the semiconductor and EDA industries into 2022.

To read the full **Semiconductor Engineering** article by **Brian Bailey**, click here.

Is Programmable Overhead Worth The Cost?

How much do we pay for a system to be programmable? It depends upon who you ask.

To read the full **Semiconductor Engineering** article by **Brian Bailey**, click here.

A Minimal RISC-V

Is there room for an even smaller version of a RISC-V processor that could replace 8-bit microcontrollers?

To read the full **Semiconductor Engineering** article by **Brian Bailey**, click here.

Industry Transforming In Ways Previously Unimaginable

As we look back over 2021, there have certainly been some surprises, but the industry continues to take everything in its stride.

To read the full **Semiconductor Engineering** article by **Brian Bailey**, click here.

The High But Often Unnecessary Cost Of Coherence

Cache coherency is expensive and provides little or negative benefit for some tasks. So why is it still used so frequently?

To read the full **Semiconductor Engineering** article by **Brian Bailey**, click here.

Release Information

riscvOVPsim and riscvOVPsimPlus - LATEST NEWS

The latest Imperas and OVP release at the Open Virtual Platforms website.

For an introduction to RISC-V the free single-core envelope model, called **riscvOVPsim**, is an excellent starting point, which can be configured for all

the ratified ISA features and includes support of the draft specifications for Bit Manipulation and Vectors.

The latest version was is available via GitHub here.

The free enhanced **riscvOVPsimPlus**, including many more features including full configurable instruction trace, GDB/Eclipse debug, and memory configuration options, plus the RISC-V Vector and other test suites, is now available on the OVP website here.

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