Imperas Newsletter – July 2021

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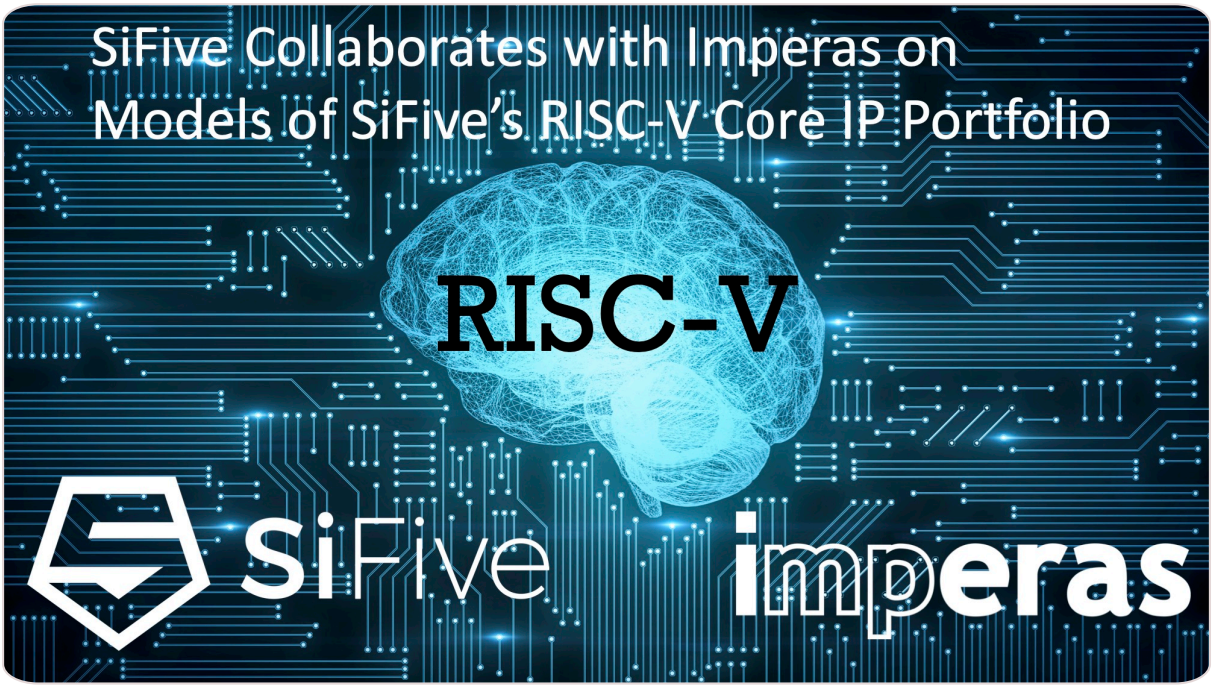
RISC-V Reference Model for Processor DV

Latest News



SiFive has qualified the Imperas models for the full range of the SiFive processor RISC-V Core IP Portfolio.

"The design freedoms of RISC-V and vector extensions are changing the traditional boundaries between the software and hardware phases of SoC development," said **Chris Jones, VP product marketing, SiFive**. "The Imperas models of the SiFive cores help developers with SoC architectural exploration across the full flexibility of the SiFive Core IP Portfolio, and support early software development, which is a critical factor in validating new AI solutions."

"SoC projects are all about partnerships; hardware and software engineers working together, with a complete ecosystem of supporters," said **Phil Dworsky, Director, Strategic Alliances, SiFive**. "With this Imperas collaboration, our mutual customers will benefit from the availability of SiFive qualified models that are compatible with the mainstream EDA tool flows."

“The SiFive Core IP portfolio covers the spectrum of the RISC-V ISA, from embedded controllers, to multiprocessors supporting SMP Linux, plus the latest vector-based accelerators,” said **Simon Davidmann, CEO, Imperas Software Ltd**. “These are the starting points for the next generation of domain-specific devices across almost all market segments and applications. Imperas is ready to support designs featuring single-core through to many-core arrays with our SiFive qualified models.”,

To read the full announcement, please click here.

For more information, please click here.

To address the rapidly expanding worldwide market for RISC-V processor verification, Valtrix Systems has signed a multi-year distribution and support agreement with Imperas. Imperas simulation technology and RISC-V reference models are now available pre-integrated within Valtrix STING for advanced RISC-V processor verification.

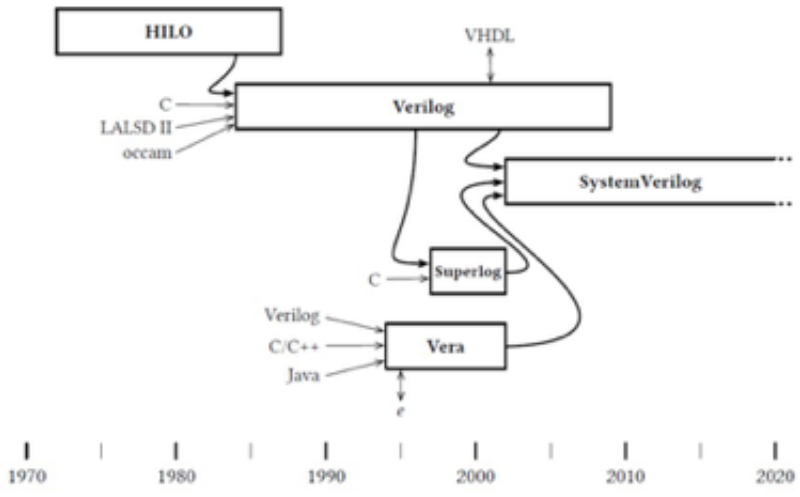
“The flexibility of RISC-V helps us address domain-specific requirements with custom processors that go beyond the roadmap of the mainstream IP providers,” said **Richard Bohn, Engineering Director at Seagate Technology, the world’s leading manufacturer of hard drives**. “Designing a high-performance RISC-V processor that achieved up to 3x the performance in critical workloads was no small feat. We needed to balance the features and options with the verification implications. The combined solution of Imperas golden reference models and Valtrix STING has helped us to achieve our verification and schedule goals.”

“Ideally any test should provide a clear pass or fail indication. In the case of RISC-V processor DV this is achieved with a comparison against a quality reference model,” said **Shubhodeep Roy Choudhury, Managing Director & Co-founder, Valtrix**. “STING helps generate portable, architecturally correct and self-checking tests targeted at the corner-case scenarios by automating the comparison of the DUT against the Imperas reference model results.”

“As SoC verification teams adapt to the complexities of DV for a RISC-V processor, we see a growing demand for efficiency as teams scale resources over multiple overlapping projects, continuous integration, and regression testing,” said **Simon Davidmann, CEO at Imperas Software Ltd**. “Having successfully worked with Valtrix in supporting many mutual customers projects, this partnership now offers a frictionless path for STING users to our simulation technology and RISC-V reference models.”

To read the full announcement, please click here.

Events



The Verilog family tree, 1972 – 2020 and beyond

HOPL IV, June 20-22

The Fourth ACM SIGPLAN History of Programming Languages Conference June 20-22 2021 is the leading conference on the history of programing languages held approximately every 10 years. At this year's conference, Simon Davidmann was co-author of the paper on Verilog and SystemVerilog.

'Verilog HDL and Its Ancestors and Descendants'
Co-author: **Peter Flake, Elda Technology Ltd**, UK

Co-author: **Phil Moorby, Rockport**, Mass., USA
Co-author: **Steve Golson, Trilobyte Systems**, USA
Co-author: **Arturo Salz, Synopsys, Inc**, USA
Co-author: **Simon Davidmann, Imperas Software Ltd**, UK

In 1997, Co-Design Automation Inc. was set up by Simon Davidmann and Peter Flake, to design and implement a new language and simulator. Phil Moorby joined in 1999. The company name showed the desire to include software/hardware co-design, but there was more customer interest in hardware design and verification, and even system specification. Their original vision of Superlog (derived from Super and Verilog) was to have a single language for system specification, hardware design, hardware verification, and software development. Superlog was later renamed to SystemVerilog as it became adopted by Accellera and later became an IEEE standard.

To download the paper, click here.

RISC-V Forum on Embedded Technologies, July 21

This next RISC-V Forum is an online event covering the latest trends and developments for Embedded Technology, which is the heart of RISC-V due to its flexible and adaptable architecture. During the Forum, Imperas will present an update and overview on the Free ISS (Instruction Set Simulator) for the OpenHW CORE-V IP Roadmap.

Getting started with the *Free* ISS for the OpenHW CORE-V IP Roadmap
Speaker: **Simon Davidmann, Imperas Software Ltd**, UK
When: July 21st 2021 @ 9:55 am China Central Time (CST), UTC +8

An ISS is a software-based representation of a processor that can be used to test and develop software on a standard host x86 PC machine. The main advantages of an ISS over a traditional hardware development platform are the ease-of-use features that help the programmer with debug, control, and visibility of code running in simulation. With new processor IP cores, the ISS is an essential tool to support the development of software before silicon or hardware

implementations are available.

The *free* OpenHW ISS can be configured for the complete range of the OpenHW CORE-V open-source processor IP portfolio, including the RTL-frozen CV32E40P (formally known as PULP RI5CY), the under-development CV32E40S and CV32E40X, plus the upcoming CVA6-32/64 bit (formally known as ARIANE).

Click here to register to attend the RISC-V Forum.

ARTICLES FROM SEMICONDUCTOR ENGINEERING
DEEP INSIGHTS FOR THE TECH INDUSTRY

Scaling Simulation
Has simulation performance stagnated, and what is the industry doing to correct it?

Pushing The Limits Of Hardware-Assisted Verification
Demand for big-iron tools is insatiable as complexity continues to grow.

Do We Have An IC Model Crisis?
Models enable automation and optimization, but today the need for new and more complex models is outstripping the ability to ratify and standardize those models.

The Lost Art Of Processor Verification
Using SoC methodologies for RISC-V processor DV.

Adding Value To Open-Source RISC-V Cores With Verification
A collaboration to verify the Open Source CV32E40P (PULP RI5CY) core using industrial grade techniques provides a set of guidelines for the community.

Release Information

OVP and riscvOVPsim RELEASE NEWS

The latest Imperas and OVP release at the Open Virtual Platforms website.

For an introduction to RISC-V the free single core envelope model, called **riscvOVPsim**, is an excellent starting point, which can be configured for all the ratified ISA features and includes support of the draft specifications for Bit Manipulation and Vectors.

The latest version was is available via GitHub here.

The free enhanced **riscvOVPsimPlus**, including many more features including full configurable instruction trace, GDB/Eclipse debug, and memory configuration options, plus the RISC-V Vector and other test suites, is now available on the OVP website here.

riscvOVPsim, learn more