Imperas Newsletter – July 2022

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The leader in RISC-V simulation solutions

News

Congratulations to the OpenHW Group on the announcement of their CORE-V MCU Dev/Kit project based on the high-quality CV32E40P open-source processor IP core, the first core to be fully verified within the OpenHW CORE-V family. This marks the first of many projects based on the CV32E40P, which was verified using the Imperas RISC-V golden reference model, now in development both within open-source community projects and commercial designs. The use of the Imperas lock-step-compare methodology for the verification of the CV32E40P now sets the standard for quality verification for RISC-V processor cores, not just open-source IP.

“OpenHW is determined to provide high-quality open-source hardware IP compatible with the established EDA tools and flows for adoption in commercial

designs," said **Simon Davidmann, CEO at Imperas Software Ltd**. "The CV32E40P as the first IP core to be completed in the CORE-V-VERIF flow marks not just the completion of a project, but the start of the era when open-source cores can be adopted in commercial designs without compromise. Research may well drive some aspects of innovation, but quality verification drives adoption."

To find out more information, please contact us or follow this link.

If you are attending this year's DAC and would like, we recommend you drop by our stand to watch Aimee Sutton's talk on this topic - scroll down for more details.

In May 2022 RISC-V International's Architectural Test SIG (formerly the compliance working group) moved to using a Python program/framework v3.0 to run compliance testing and no longer provides signatures or scripts to run targets against their tests. As a service to RISC-V processor developers, Imperas has ported the RVI tests to the Imperas test framework and makes them available for free with **riscvOVPsimPlus** as part of the Imperas test downloads. This means you can use all of the Imperas tests and all of the RVI tests from one simple make/bash framework. The RISC-V International tests have the -RVI suffix.

"With all the design freedoms that RISC-V offers, verification has never been more important to ensure full ecosystem support for new processor implementations," said **Simon Davidmann, CEO at Imperas Software Ltd**. "The best test for a processor is simulation-based testing to verify the

interaction between the software program and the hardware operation. Architectural Validation test suites, while not a complete verification plan, offer the basic confirmation necessary to sustain the ecosystem of software support. We are pleased to offer the latest suites for the key ratified specifications of Vectors, Bit Manipulation and Crypto plus the new Embedded E suite, all for free including commercial use, with riscvOVPsimPlus."

For further details, please contact us or follow this link.

Together, leveraging their proven expertise in processor simulation and system verification respectively, Imperas and Breker plan to develop interfaces and standards to unify the functional verification design flows to enable DV teams to improve efficiency and verification IP reuse across the complete verification process from plan to silicon prototype.

"RISC-V represents an inflection point for semiconductor verification as the design freedoms provided by the open ISA means an assumption of the responsibility of the processor and system verification task," said **David Kelf, CEO at Breker Verification Systems**. "In partnering with Imperas, the leaders in RISC-V processor verification, we can offer a combination of technologies and interface standards for IP and SoC testing that ensures commercial-grade verification for these flexible devices right through to the end platform."

"RISC-V marks the end of the one-size-fits-all approach to processor IP, now all SoC developers can explore new innovations with processor IP configured for the target application," said **Simon Davidmann, CEO at Imperas Software**

Ltd. “Many of our customers are exploring the design side possibilities of new processor architectures and their implications for SoCs and systems in parallel, extending the verification scope from IP cores to system-level integration. With Breker’s proven system verification experience, we are streamlining the critical verification tasks to enable the full potential of RISC-V based devices with commercial-grade verified quality.”

If you are attending this year's DAC, please stop by and see the latest developments for RISC-V Verification, see **Breker at booth #2528** and **Imperas at #2336**, and also in the OpenHW pavilion at #2340.

For further details, please contact us or follow this link.

Upcoming Events

Imperas will be at DAC 2022 in San Francisco, which runs from **July 10-14, 2022,** with presentations and exhibition booths #2336 and #2340. For more information, or to schedule a demonstration session at DAC 2022, please contact us via info@imperas.com.

During the DAC 2022 conference, Imperas will participate in the following panel sessions and talk:

Panel: Those Darn Bugs! When Will They be Exterminated for Good?
The question many DAC attendees ask is whether bug eradication will ever become a reality. The panel will explore this topic in detail to find out what’s

causing the industry to not scale verification to the point that we can sign off our chips on time, the first time with zero bugs.

Who: Ashish Darbari - **Axiomise**
Mark Glasser - **Cerebras**
Ty Garibay - **Mythic AI**
Simon Davidmann - **Imperas**
Moderator: Brian Bailey - **Semiconductor Engineering**
When: Monday July 11, 3:00pm-3:45pm PDT
Where: DAC Pavilion (Room #2260, Level 2)

Panel: RISC-V: Open and Flexible, but still a Standard?

This panel will explore 'how well has RISC-V performed as an open standard ISA that encourages innovation without chaos and fragmentation?'

Who: Himanshu Sanghavi (Organizer) - **Meta**
Pierre Selwan - **Microchip**
Yunsup Lee - **SiFive**
Charlie Cheng - **Andes**
Larry Lapides - **Imperas**
Jim Wang - **Meta**
Moderator: Edward Sperling - **Semiconductor Engineering**
When: Wednesday July 13, 1:30pm-3:00pm PDT
Where: Engineering IP Track (Room #2012, Level 2)

Talk: RISC-V Models for Verification, Software Development and Architectural Exploration

As RISC-V processors start to be used more and more in SoCs, the industry needs to look beyond the RISC-V ISA to the requirements for use. These include a well-verified implementation, the ability to develop, debug and test software, especially early in the project, and the need to explore different implementations, including different processors, multi-hart processors and custom instructions. One common element of these requirements is a high-quality model of the RISC-V cores being used.

This presentation will report on the test-driven development methodology used to build the Open Virtual Platforms (OVP) models of RISC-V cores (~100 different cores available in the OVP Library and provided to processor IP developers), and show how these models have been used for design verification, software development and architectural exploration.

Specifically, this presentation will discuss how the availability of high-quality

models of RISC-V processors impacts the design process, including in design verification (DV), software development and architecture exploration. This talk will show examples of industry uses of these models for those use cases, including step-and-compare DV flows, software and operating system porting and bring up, and analysis and optimization of custom instructions.

Speaker: Larry Lapides – **Imperas**
When: Tuesday July 12, 1:30pm-2:15pm PDT
Where: Open-Source Central Theater #2338

Talk: Introduction to RISC-V Verification with new open standard RVVI (RISC-V Verification Interface)

As an open standard ISA, RISC-V has attracted the attention of system designs, hardware engineers and software developed based on the new freedoms for design optimizations. The OpenHW Group has been formed by members looking to build on the potential of open-source hardware IP as a foundation for further extensions and adoption in mainstream commercial designs. With this surge in design innovation, the challenge for the verification task is not just the complexities of modem processor design innovations, but the scale of projects as the DV task moves from a few specialist providers to all adopters that chose to exploit the full potential now available with RISC-V for optimized processors in domain-specific applications.

This talk will highlight the key aspect of a RISC-V verification plan based on the pioneering work at OpenHW to deliver quality open-source IP cores with industrial-strength verification for adoption in the established commercial tools and design flows. With a case study around the CV32E40P as an example of the latest methods of 'lock-step-compare' for asynchronous events and debug operations. The new open standard of RVVI (RISC-V Verification Interface) supports the full flexibility of RISC-V for designs with privilege modes, vectors, out-of-order pipelines, multi-threading, multi-heart, plus user-defined custom instructions and extensions.

Speaker: Aimee Sutton – **Imperas**
When: Monday July 11, 2:30pm-3:15pm PDT
Where: Open-Source Central Theater #2338

For more information and registration please visit DAC 2022.

ARTICLES FROM SEMICONDUCTOR ENGINEERING
DEEP INSIGHTS FOR THE TECH INDUSTRY

Who Does Processor Validation?

Defining what a processor is, and what it is supposed to do, is not always as easy as it sounds. In fact, companies are struggling with the implications of hundreds of heterogenous processing elements crammed into a single chip or package. Companies have extensive verification methodologies, but not for validation...

To read the full **Semiconductor Engineering** article by **Brian Bailey**, click here.

IC Reliability Burden Shifts Left

Chip reliability is coming under much tighter scrutiny as IC-driven systems take on increasingly critical and complex roles. So whether it's a stray alpha particle that flips a memory bit, or some long-dormant software bugs or latent hardware defects that suddenly cause problems, it's now up to the chip industry to prevent these problems in the first place, and solve them when they do arise...

To read the full **Semiconductor Engineering** article by **Ann Steffora Mutschler**, click here.

Why Hardware-Dependent Software Is So Critical

Hardware and software are two sides of the same coin, but they often live in different worlds. In the past, hardware and software rarely were designed together, and many companies and products failed because the total solution was unable to deliver. The big question is whether the industry has learned anything since then...

To read the full **Semiconductor Engineering** article by **Brian Bailey**, click here.

IP Industry Transformation

The IP market already has witnessed a sweeping shift from a “design once, use everywhere” approach, to an “architect once, customize everywhere” model, in which IP is highly configurable and customizable and the focus is on domain-specific optimization. But as chips become increasingly complex, and as new types of IP and licensing models continue to gain ground — especially on the processor side with RISC-V — more changes are coming...

To read the full **Semiconductor Engineering** article by **Brian Bailey**, click here.

Release Information

riscvOVPsim and riscvOVPsimPlus - LATEST NEWS

The latest Imperas and OVP release at the Open Virtual Platforms website.

For an introduction to RISC-V the free single-core envelope model, called **riscvOVPsim**, is an excellent starting point, which can be configured for all the ratified ISA features and includes support of the latest ratified specifications including Bit Manipulation, Crypto (scalar) and Vectors.

The latest version is available via GitHub here.

The free enhanced **riscvOVPsimPlus**, including many more features including full configurable instruction trace, GDB/Eclipse debug, and memory configuration options, plus the RISC-V Vector and other test suites, is now available on the OVP website here.

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