Imperas Newsletter – June 2021



imperas

RISC-V Reference Model for Processor DV

## Latest news


# Imperas Simulation Reference Models selected by IAR Systems for Arm 64bit

**IAR Systems has selected the Imperas ARM model AArch64 Armv8-A as the simulator technology for the development toolchain IAR Embedded Workbench for Arm.**

For embedded developers, the IAR Embedded Workbench with integrated Imperas simulator provides a rapid test and development environment to compile, debug and analyze code without the need for external hardware or boards. The Imperas models cover the envelope of the Arm V8-A Architecture and can be configured to represent any core or implementation.

“64bit is not just about the word length or address space of a processor,” said **Anders Holmberg, General Manager Embedded Development Tools, IAR Systems**. “The Arm v8 cores offer embedded developers a step-change in performance and capability, this potential is now complemented with high-performance simulation software. Software developers can migrate to the latest devices with confidence based on the IAR Systems development tools and Imperas simulator technology.”

“Embedded developers by definition develop firmware, software and applications that are tightly optimized to the underlying hardware,” said **Simon Davidmann, CEO at Imperas Software Ltd**. “Imperas is pleased to provide the quality reference models that enable IAR Embedded Workbench users to get the best from the latest generation of Arm v8 based devices.”

**Learn more**

## Events


### CadenceLIVE Americas, June 8-9

Imperas is participating at the online virtual event highlighting the latest advances for UVM RISC-V Verification with RISC-V Processor Reference Models and SystemVerilog.

**‘The Step-and-Compare methodology for high-quality RISC-V processor verification’**

- Co-author: Simon Davidmann – Imperas
- Co-author: Lee Moore – Imperas
- When: June 9th 11:25 am PDT

This talk introduces the various options for RISC-V processor verification from the simple trace analysis through to the latest techniques with test benches that support UVM SystemVerilog with Step-and-Compare for asynchronous events. With illustration of the various options and approaches including details of bugs found on some popular open-source cores.

**'The open verification method used by OpenHW for the CV32E40P RISC-V core'**

- Co-author: Mike Thompson – OpenHW
- Co-author: Lee Moore – Imperas
- When: June 8th 10:15 am PDT

This talk explores the background, development and implementation of the OpenHW verification environment for CV32E40P known as "core-v-verif". Since the goal of the project is to support the adoption of an open-source core, the initial deliverable quality is not the only concern. One attractive aspect of an open-source core is the potential for adopters to modify, adapt, or extend the base core features. Thus, the verification plan needs to anticipate the future use case with flexibility built-in and clear documentation.

For more information about the CadenceLIVE Americas, visit the event website.

**Discover more**

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## RISC-V World Conference China, June 22-24

Imperas will participate in the first RISC-V World Conference in China which will be hosted at Shanghai Tech University from June 22 to 24, 2021.

### 'RISC-V Reference Models for Verification, Software Development and Architectural Exploration'

- Speaker: Katherine (Kat) Hsu – Imperas
- Co-author: Lee Moore – Imperas
- When: TBD

This talk will report on the test-driven development methodology used to build the Open Virtual Platforms (OVP) open-source models of RISC-V cores, and show how these models have been used for design verification, software development and architectural exploration.

### 'RISC-V Reference Models for Verification, Software Development and Architectural Exploration'

- Speaker: Kevin McDermott – Imperas
- When: TBD

This presentation will review the five different DV flows, from signature comparison to trace comparison to step-and-compare, and discuss the tradeoffs in effort, completeness and cost between the flows.

### 'Case study: The open verification flow for the CV32E40P open source RISC-V IP Core'

- Speaker: Kevin McDermott – Imperas
- When: TBD

This case study explores the background, development and implementation of the OpenHW verification environment for CV32E40P known as "core-v-verif". The verification plan needs to anticipate the future use case with flexibility built-in and clear documentation.

For more information about the RISC-V World Conference China 2021, visit the event website.

**Find out more**

## Videos


## RISC-V Processor Verification: Case study

This YouTube video is a recording of a technical paper presented at DVCon 2021. This video recording features a presentation that reports on the techniques used and lessons learned for the verification of an RV64IMACBNSU RISC-V processor by an experienced SoC design team, including the development of the reference model and the SystemVerilog and C encapsulation of the reference model, the step-and-compare flow used included co-debug, and the Specman-based verification environment.

**Watch video**

**Download slides**

**Read technical paper**

## Articles

SEMICONDUCTOR ENGINEERING
DEEP INSIGHTS FOR THE TECH INDUSTRY

# New Methodologies Create New Opportunities

*Does RISC-V processor verification provide common ground to develop a new verification methodology, and will that naturally lead to new and potentially open tools?*

· BY: **BRIAN BAILEY**

SOME MORE ARTICLES FROM SEMICONDUCTOR ENGINEERING
DEEP INSIGHTS FOR THE TECH INDUSTRY

## Roadblocks For ML In EDA

Successful utilization of machine learning within EDA cannot happen without confidence in the quality of results. That presents challenges. Read more.

## Standards, Open Source, And Tools

EDA has been more successful creating open languages and standards rather than promoting open-source collaboration. Will this change? Read more.

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## Imperas Blog: Getting Started with RISC-V

## Verification

An article highlighting Design Verification (DV) test planning using a trusted SoC methodology for RISC-V processor verification including custom extensions [Read more](#).

# Release information

### OVP and riscvOVPsim RELEASE NEWS

The latest Imperas and OVP release at the [Open Virtual Platforms website](#).


For an introduction to RISC-V the free single core envelope model, called riscvOVPsim, is an excellent starting point, which can be configured for all the ratified ISA features and includes support of the draft specifications for Bit Manipulation and Vectors.

The latest version was uploaded on 29 March 2021, Version: 20210329.0 and is available via [GitHub here](#).

The free enhanced riscvOVPsimPlus, including many more features including full configurable instruction trace, GDB/Eclipse debug, and memory configuration options, plus the RISC-V Vector and other test suites, is now available on the [OVP website here](#).

**riscvOVPsim, learn more**