Imperas Newsletter – June 2022

The leader in RISC-V simulation solutions

News

NSITEXE Selects ImperasDV for Automotive Quality RISC-V Processor Functional Design Verification

NSITEXE, Inc., a group company of the DENSO Corporation that develops and sells high-performance semiconductor IP for automotive applications, has selected **ImperasDV** for advanced RISC-V processor hardware design verification.

"The flexibility of the RISC-V ISA coupled with the performance of vector extensions is an ideal starting point for AI accelerators for automotive

applications," said **Hideki Sugimoto, CTO of NSITEXE, Inc., a group company of DENSO Corporation**. "To address the verification requirement for our next generation of processors, we have developed an optimized verification flow with **ImperasDV** that our design team set up with detailed configuration options to deliver on their comprehensive verification plans that provides the industry leading quality our customers expect."

To find out more information, please follow this link.

Upcoming Events

Imperas will participate at Embedded World 2022 in Nuremberg, Germany, which runs from **June 21-23, 2022**.

Stop by the RISC-V booth in Hall 1 location 1-550 and see all the latest Imperas simulation technology for RISC-V, including advanced RISC-V processor verification, virtual prototypes, software development and custom instruction, plus support for the latest ratified RISC-V specifications including vector accelerators and draft extensions included with the Imperas reference model for RISC-V.

For more information, or to set up meetings with Imperas at the Embedded Word 2022, please contact info@imperas.com.

The RISC-V Theatre will also feature the following talks by Imperas during the Embedded World Conference:

Introduction to RISC-V Processor Verification

Speaker: Larry Lapides – Imperas Software
Co-Author: Lee Moore – Imperas Software
When: Tuesday June 21: 10:00am CEST

The open RISC-V Instruction Set Architecture (ISA) is enabling a wide range of options on the design side, to complement this a number of options can be applied to the verification tasks, since a basic proof of concept prototype may not need all the quality checks as a high volume or high-reliability application.

This talk will review the 5 different simulation-based DV flows, ranging from simple signature-based comparisons for architectural validation to advanced 'step-and-compare' flows that support asynchronous events and debug.

Running Quake on RISC-V with virtual platforms

Speaker: Kevin McDermott – Imperas Software
Co-Author: Simon Davidmann – Imperas Software
When: Wednesday June 22: 11:30am CEST

While much of the focus and energy of the RISC-V adopters has so far gone into the development of the RISC-V architecture and specific cores, the real success of RISC-V is dependent upon the key software tasks for new applications, porting legacy software, and optimizing OS/RTOS ports and drivers for the wide range of RISC-V devices being built. With more custom silicon projects starting every day, virtual platforms (often called virtual prototypes) offer a viable alternative to hardware prototypes for software engineering tasks. This talk will highlight how simulation and virtual platforms can be used for software development for new processors and SoCs including a demonstration with Quake running on RISC-V.

Getting started with RISC-V custom instructions

Speaker: Larry Lapides – Imperas Software
Co-Author: Duncan Graham – Imperas Software
When: Thursday June 23: 1:30pm CEST

One of the attractive features of RISC-V is the ability to add, while maintaining ecosystem software support, new optimized instructions and extensions to a processor implementation. At first, it appears a simple task to look at opportunities in the application code that could be accelerated with some dedicated new hardware. However, since hardware typically has a much longer life cycle than software, future updates and roadmap needs must be anticipated. Thus, the art of ISA design is using fine-grain analysis to accelerate just the key steps while leaving sufficient flexibility to support new software updates and advances. Also, in multi-core arrays, the use of custom extensions can offer a lightweight communication channel between processors. This extends the scope beyond the processor itself into system design and analysis. This talk will illustrate the key profiling and analysis steps for custom extensions and optimization.

For more information and registration please visit Embedded World 2022.

Imperas will be at DAC 2022 in San Francisco, which runs from **July 10-14, 2022**.

Stop by the Imperas booth (2336) or our pod on the OpenHW stand (2245-F) to see all the latest demonstrations of **ImperasDV** for RISC-V processor verification, plus virtual platforms for software development.

For more information, or to schedule a demonstration session at DAC 2022, please contact the Imperas team via info@imperas.com.

During the DAC 2022 conference, Imperas will participate in the following panel sessions:

Those Darn Bugs! When Will They be Exterminated for Good?

Who:	Ashish Darbari - Axiomise
	Mark Glasser - Cerebras
	Ty Garibay - Mythic AI
	Simon Davidmann - Imperas
Moderator:	Brian Bailey - Semiconductor Engineering
When:	Tuesday July 12, 2:00pm-2:45pm PDT
Where:	DAC Pavilion

The question many DAC attendees ask is whether bug eradication will ever become a reality. The panel will explore this topic in detail to find out what's causing the industry to not scale verification to the point that we can sign off our chips on time, the first time with zero bugs.

RISC-V: Open and Flexible, but still a Standard?

Who: Himanshu Sanghavi (Organizer) - Meta
                 Pierre Selwan - Microchip
                 Yunsup Lee - SiFive
                 Charlie Cheng - Andes
                 Larry Lapides - Imperas
                 Jim Wang - Meta
Moderator: Edward Sperling - Semiconductor Engineering
When: Wednesday July 13, 1:30pm-3:00pm PDT
Where: Engineering Tracks, IP

This panel will explore 'how well has RISC-V performed as an open standard ISA that encourages innovation without chaos and fragmentation?'

For more information and registration please visit DAC 2022.

Video Content

Gabriele Saucier, CEO at Design & Reuse, interviews **Larry Lapides** at IP-SoC 2022.

Big Changes In Embedded Software

Every good hardware or software design starts with a structured approach throughout the design cycle, but as chip architectures and applications begin focusing on specific domains and include some version of AI, that structure is becoming more difficult to define. Embedded software, which in the past was written for very narrow functions with a minimal footprint, is increasingly getting blended into the overall system design and re-used wherever possible….

To read the full **Semiconductor Engineering** article by **Ann Steffora Mutschler**, click here.

Choosing Which Tasks To Optimize In Chips

Just a few years ago, most people were happy to buy processors from the likes of Intel, AMD and Nvidia, and IP cores from Arm. Some even wanted the extensibility that came from IP cores like Tensilica and ARC. Then, in 2018, John Hennessy and David Patterson delivered the Turing Lecture titled "A New Golden Age for Computer Architecture: Domain-Specific Hardware/Software Co-Design, Enhanced Security, Open Instruction Sets, and Agile Chip Development." While it was not the lecture that started the drive towards more optimization, it certainly elevated it to the global consciousness…

To read the full **Semiconductor Engineering** article by **Brian Bailey**, click here.

The Challenges Of Incremental Verification

In the design flow, tools and methodologies have been created to minimize the chance of problems, particularly as you approach tape-out, by making safe, non-optimal corrections. But there are no such tools or methodologies for verification. "You have tons of resources focused on verification," says **Simon Davidmann, founder and CEO of Imperas Software**. "The goal is to minimize what design changes you make because with the technologies that are available today, when you change something in the design, you need to rerun everything…

To read the full **Semiconductor Engineering** article by **Brian Bailey**, [click here](#).

[Embedded Software: Sometimes Easier, Often More Complex](#)

From a conceptual level, the general definition of embedded software has not changed much. It's still low-level drivers and RTOSes that run close to the hardware, deterministic in nature, and time- and resource-critical. But the ecosystem around that software and the methodologies used to create it have changed significantly….

To read the full **Semiconductor Engineering** article by **Ann Steffora Mutschler**, [click here](#).

[How To Optimize A Processor](#)

Optimizing any system is a multi-layered problem, but when it involves a processor there are at least three levels to consider. The first level of potential optimization is at the system level. For example, how does data come in and out of the processing cores? The next level is the architecture of the processing cores themselves. This may involve adopting an existing processor or adding instructions to an extensible core. The final level of optimization is the micro-architectural level. This is where implementation pipelines are defined…

To read the full **Semiconductor Engineering** article by **Brian Bailey**, [click here](#).

Release Information

[riscvOVPsim and riscvOVPsimPlus - LATEST NEWS](#)

The latest Imperas and OVP release at the [Open Virtual Platforms website](#).

For an introduction to RISC-V the free single-core envelope model, called **riscvOVPsim**, is an excellent starting point, which can be configured for all the ratified ISA features and includes support of the latest ratified specifications including Bit Manipulation, Crypto (scalar) and Vectors.

The latest version is available via GitHub here.

The free enhanced **riscvOVPsimPlus**, including many more features including full configurable instruction trace, GDB/Eclipse debug, and memory configuration options, plus the RISC-V Vector and other test suites, is now available on the OVP website here.

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