IMPERAS TO DEMONSTRATE VIRTUAL PLATFORMS, TOOLS AND RISC-V VERIFICATION REFERENCE MODELS AT DVCON 2020 IN SAN JOSE

We will participate in the DVCon Conference and Exhibition, March 2-5 2020 at the Double Tree Hotel, San Jose, California. We'll be showcasing our latest verification solutions including the recently announced reference model with UVM encapsulation for RISC-V verification and a new collaboration with Mentor on the latest hardware Design Verification (DV) flow for RISC-V processor implementations.

As well as exhibiting on booth #1001 you can see us present a technical paper and participate in a panel discussion:

· "Rolling the dice with random instructions is the safe bet on RISC-V verification" – by Simon Davidmann, CEO Imperas
Tuesday March 3, track session 3:00pm – 5:00pm

The traditional SoC verification approach has until now been based on the fundamental assumption of known good processor IP from the mainstream semiconductor IP providers. With Open ISAs such as RISC-V, developers can exploit a greater degree of implementation flexibility, but must also assume a greater role in the verification task. To complement the established technique,

this paper illustrates the approach using an open-source random instruction generator for RISC-V with a cloud-based environment for capacity flexibility, to compare implementation RTL against a reference simulation model. This latest framework covers the needs of specialist core designers and all SoC adopters.

· **"New chip designs create tidal wave of change" – panelist Simon Davidmann, CEO Imperas**
Wednesday March 4, 8:30am – 9:30am

DVCon attendees are invited to attend a Town Hall discussion on the need for a more thorough verification methodology as complexity converges with open source initiatives such as RISC-V.

For more information or to meet with someone from the team to discuss RISC-V reference models for processor verification and compliance, including draft specifications for Vectors and Bit Manipulation at DVCon, please get in touch here.
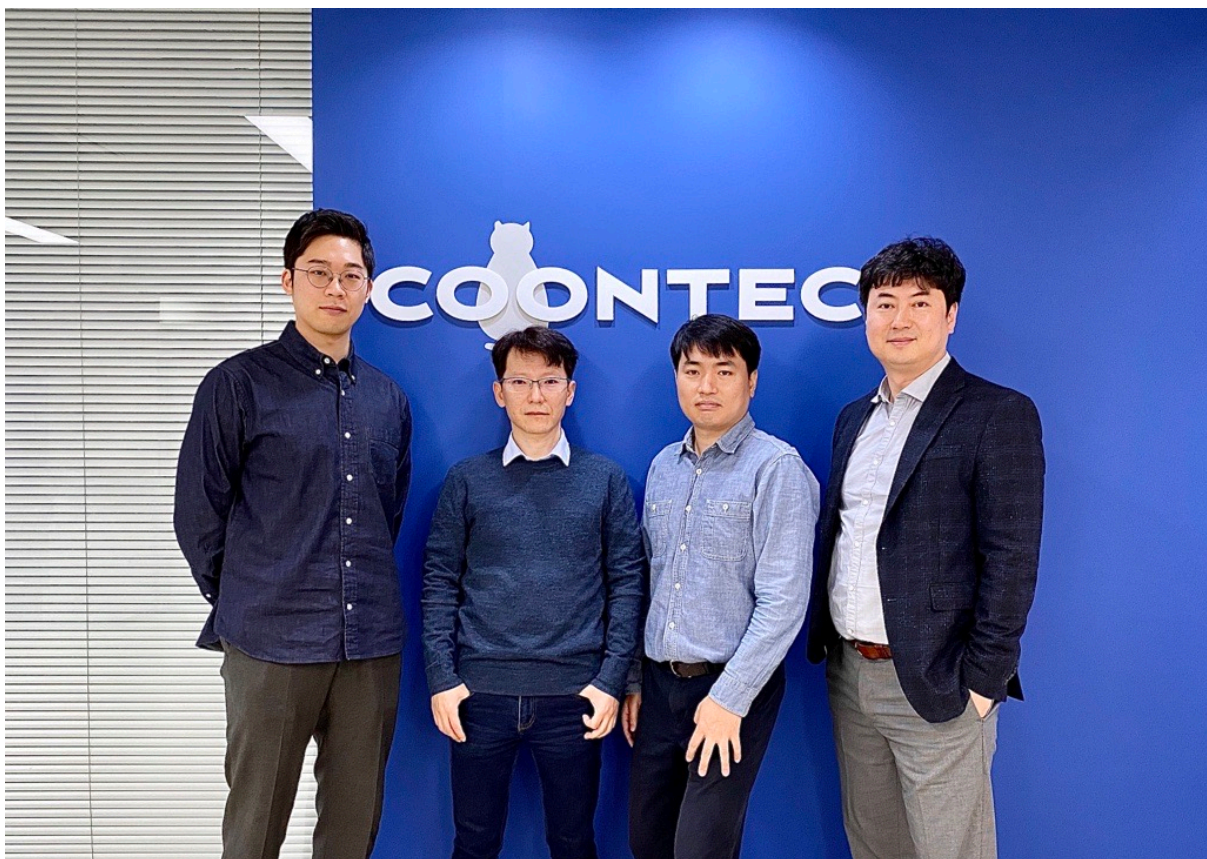
Imperas appoints Coontec as its Certified Design and Verification Partner supporting Leading Edge SoC Designs in South Korea

Today we announced the certification of Coontec Design Center based in Pangyo Techno Valley, South Korea. The extensive partnership will provide customers with virtual platform design services to accelerate early stage software development and hardware verification schedules.

Virtual platforms offer advantages over hardware prototypes with early availability and flexibility. Software models of the key components in a processor platform are combined to form an executable sub-system. The models must have enough functionality to execute the code correctly, but retain a level of abstraction that

provides the performance necessary for rigorous testing.

Heterogeneous designs and many-core processor arrays are typical of the design structures in development for the next generation AI (Artificial Intelligence) and ML (Machine Learning) designs.
With demanding workloads based on real-world datasets, a virtual platform approach allows the opportunity to fine-tune the hardware structure and software algorithms to find the optimum configuration. Also in many IoT applications, a total system level design approach is required to model arrays of deployed nodes as digital twins. The use of virtual platforms permits a system wide view to configure and optimize all levels of the hardware and software. Working closely with system architects and developers, virtual platform development engineers provide the key bridge between the hardware and software teams in the early phase of a project, and become the essential reference for pre-tape-out hardware verification testing, and a more comprehensive source of software testing in production.

"Coontec provides flexible services to help and assist engineering projects, with services that can be customized as required to provide support, training and consultancy as well as expert resources for turnkey projects," said **Joon Pang, CEO of Coontec.** "Using the OVP modeling infrastructure allows open-source models and virtual platforms that give customers options in managing projects with flexible combinations of internal and external teams."

"When our research teams look at the next generation of designs for IoT, ML and AI, the use of the full application workload and real-world datasets is key to exploring architectural options with virtual platforms," said **Han Jin Cho, Executive Director, ETRI Korea.** "The Imperas virtual platform based methodology, coupled with the services provided by the Coontec team, provides the Korean market with additional flexibility and capabilities with locally based and trusted expert resources."

"As virtual platforms become more critical to our customers projects for system level architectural exploration, software development and hardware verification – the one limitation customers report is the availability of local expert consultancy services," said **Larry Lapides, Vice President of Sales at Imperas.** "The Imperas leading commercial tools and open source models are now complemented with Coontec professional design services."

For more information about Imperas, please see www.imperas.com. Follow Imperas on LinkedIn, twitter @ImperasSoftware and YouTube.

Or get in touch directly via info@imperas.com