Imperas Newsletter – Mar. 2023

View this email in your browser

imperas

The leader in RISC-V simulation solutions

Headline News

ImperasDV™ verification solutions are now certified for use with Synopsys functional simulation and debug tools with ‘lock-step-compare’ for RISC-V processor verification.

“RISC-V adoption is growing across key market segments as SoC teams explore the flexibility of an open standard ISA for optimized processors,” said **Kiran Vittal, senior director of Partner Alliances Marketing for Synopsys EDA Group**. “Our collaboration with Imperas, leveraging Synopsys’ leading simulation and debug solutions, enables our mutual customers to address verification complexities for RISC-V processor cores and quickly achieve

coverage convergence.”

To find out more, follow this link.

Imperas RISC-V reference models, simulator, tests, and verification IP are supporting Ventana Micro in delivering a performance-leading family of data center class CPU cores.

“At Ventana, our teams of developers are building the foundational processor IP and chiplet building blocks that will enable a step change in performance for the most demanding compute workload markets,” said **Josh Scheid, Head of Design Verification at Ventana Micro Systems Inc**. “Our verification strategy is to exercise the RISC-V based processors across the most demanding scenarios and are using Imperas RISC-V vector test suites in addition to the Imperas golden reference model in our verification environment.”

To find out more, follow this link.

Videos

Imperas and Andes recently co-hosted a webinar on optimizing a RISC-V processor with custom instructions and extensions.

At the end of the formal remarks, the presenters answered questions submitted by attendees. To read the transcript of the Q&A, click here, or to listen to the audio, click here.

Upcoming Events

Embedded World Exhibition and Conference, March 14-16 2023
Imperas will be at Embedded World 2023 in Nuremberg, Germany, demonstrating solutions for RISC-V processor verification, software development with virtual prototypes and extensions with custom instructions in conjunction with debug and analysis tools and solutions to accelerate embedded software development. Imperas are co-sponsors of the RISC-V Pavilion located in Hall 4A stand 4A-620 and will also participate in the following talks:

Conference Paper:
Advanced methodologies to address RISC-V verification for all adopters

Speaker: Jon Taylor – Imperas Software
Co-authors: Mike Thompson – OpenHW Group
Kevin McDermott – Imperas Software
Simon Davidmann – Imperas Software
Lee Moore – Imperas Software
When: Wednesday, March 15, 2023: Session 9.2 – 2:15pm (CET)

Conference Paper:
New ecosystem leads RISC-V mainstream adoption with innovation ready software development and processor verification tools
Speaker: Larry Lapides – Imperas Software
Co-authors: Mike Thompson – OpenHW Group
Davide Schiavone – OpenHW Group
Kevin McDermott – Imperas Software
Simon Davidmann – Imperas Software
When: Thursday, March 16, 2023: Session 9.3 - 12:00pm (CET)

Conference Paper:
Example of Extending RISC-V for AI/ML Domain Specific Processors
Speaker: Larry Lapides – Imperas Software
Co-authors: Pascal Gouedo – Dolphin Design
Damien Le Bars – Dolphin Design
Olivier Montfort – Dolphin Design
Mike Thompson – OpenHW Group
Kevin McDermott – Imperas Software
Lee Moore – Imperas Software
Aimee Sutton – Imperas Software
When: Thursday, March 16, 2023: Session 9.3 - 4:00pm (CET)

RISC-V Theatre:
Introduction to RISC-V Processor Verification
Speaker: Larry Lapides – Imperas Software
Where: RISC-V Pavilion in Hall 4A stand 4A-620
When: Tuesday, March 14, 2023: 10:30am (CET)

RISC-V Theatre:
Getting started with RISC-V custom instructions
Speaker: Jon Taylor – Imperas Software
Where: RISC-V Pavilion in Hall 4A stand 4A-620
When: Wednesday, March 15, 2023:10:00am (CET)

Stop by the RISC-V Pavilion (Hall 4A stand 4A-620) to see all the latest Imperas simulation technology for RISC-V, including advanced RISC-V processor verification, virtual prototypes, software development and custom instruction, plus support for the latest ratified RISC-V specifications including vector accelerators and draft extensions included with the Imperas reference model for RISC-V.

For more information, please follow this link, or to set up meetings with Imperas at the Embedded World 2023, please contact: info@imperas.com

---

DVCon 2023 Post Show Materials

Hello from DVCon 2023! During the event, Imperas presented a joint conference paper with OpenHW, and an in-depth tutorial on the latest simulation-based RISC-V processor verification techniques.

Conference paper:
The Evolution of RISC-V Processor Verification: Open Standards and Verification IP

This paper describes the evolution of RISC-V processor verification methodology using CORE-V-VERIF as a case study. The current generation uses RISC-V processor verification IP enabled by the open standard RISC-V Verification Interface (RVVI) to realize a comprehensive verification methodology that encompasses asynchronous peripheral events that occur randomly during program execution.

Co-authors: Aimee Sutton, Imperas Software
Lee Moore, Imperas Software
Mike Thompson, OpenHW Group

Follow the link to download the conference paper and presentation slides.

Workshop:

Understanding the RISC-V Verification Ecosystem

This workshop will help you understand and navigate the RISC-V verification ecosystem. Some of the topics covered include:

- Understanding the tools used in RISC-V processor verification: instruction set simulators, processor reference models, random instruction stream generators, verification IP
- Compare and contrast techniques that can be used for RISC-V processor verification: post-simulation trace compare, self-checking tests, lockstep co-simulation, functional coverage
- Open standards for RISC-V processor verification: RISC-V Verification Interface (RVVI)
- Open-source examples and commercial offerings

Presenters: Aimee Sutton, Imperas Software
Simon Davidmann, Imperas Software

To download a copy of the presentation, click here.

Articles

The RISC-V Verification Interface (RVVI) – test infrastructure and methodology guidelines

This paper contains background information and an introduction to the RISC-V Verification Interface (RVVI), an open standard that supports the flexibility of RISC-V while enabling reusable verification IP, detailed processor DV methodology, and guidelines. If you are planning your first RISC-V project, already have one in development, or want to enhance the flow from a prior project, you should consider how RVVI can increase the quality and reusability of your verification investment.

To read the full **Verification Horizons** article by **Aimee Sutton, Lee Moore, and Kevin McDermott of Imperas Software**, click here.

[*Please note: A log-in is required to read the article in full*]

Simplifying Design Verification for Increasingly Custom RISC-V Processors

RISC-V is known as an open-standard instruction set architecture (ISA) whose base instructions have been frozen to minimize complexity. But more recently it has added a wide range of custom extensions and enhancements that are making it increasingly popular amongst SoC designers building application-specific systems...

To read the full **Embedded Computing Design** article by **Brandon Lewis**, click here.

RISC-V Summit 2022: All Your CPUs Belong to Us

At the recent RISC-V Summit organized by RISC-V International, the

consortium that manages and promotes the RISC-V Instruction Set Architecture (ISA), its president, Calista Redmond, had a far more blunt message: RISC-V is inevitable...

To read the full **EETimes** article by **Kevin Krewell**, click here.

5 Takeaways From The RISC-V Summit

After an intense week at the 2022 RISC-V Summit in San Jose, California, I am fueled with energy and positive thoughts. I had plenty of time to reflect on the event, which was unique in many ways. A lot happened in a few days for us at Codasip as well as for the wider RISC-V community, and here are 5 things I will remember from this conference...

To read the full **Semiconductor Engineering** article by **Lauranne Choquin at Codasip**, click here.

Leveraging Chip Data To Improve Productivity

The semiconductor ecosystem is scrambling to use data more effectively in order to increase the productivity of design teams, improve yield in the fab, and ultimately increase reliability of systems in the field...

To read the full **Semiconductor Engineering** article by **Ann Mutschler**, click here.

How To Build Resilience Into Chips

Disaggregating chips into specialized processors, memories, and architectures is becoming necessary for continued improvements in performance and power, but it's also contributing to unusual and often unpredictable errors in hardware that are extremely difficult to find...

To read the full **Semiconductor Engineering** article by **Ed Sperling & Ann**

Mutschler, click here.

Release Information

riscvOVPsim and riscvOVPsimPlus - LATEST NEWS

The latest Imperas and OVP release at the Open Virtual Platforms website.

For an introduction to RISC-V the free single-core envelope model, called **riscvOVPsim**, is an excellent starting point, which can be configured for all the ratified ISA features and includes support of the latest ratified specifications including Bit Manipulation, Crypto (scalar) and Vectors.

The latest version is available via GitHub here.

The free enhanced **riscvOVPsimPlus**, including many more features including full configurable instruction trace, GDB/Eclipse debug, and memory configuration options, plus the RISC-V Vector and other test suites, is now available on the OVPworld website here.

Has someone forwarded our newsletter to you? Join our mailing list.