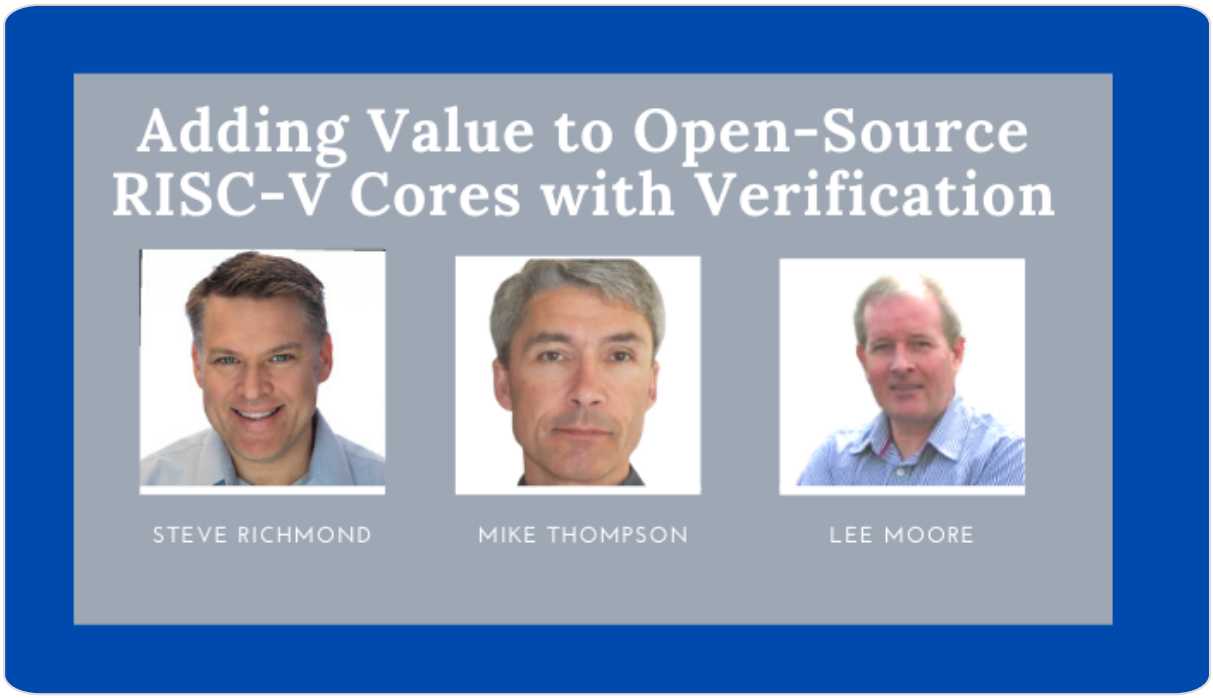
imperas

RISC-V Reference Model for Processor DV

Feature article

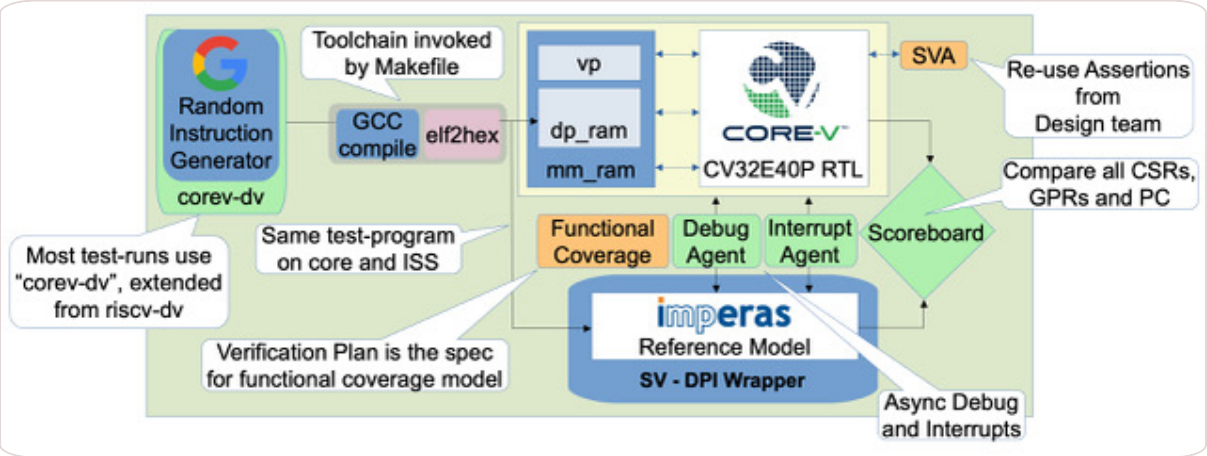


Modern SoC verification has matured to the point that some are suggesting the use of the word 'prototype' when referring to the first silicon samples is now unnecessary. This is due in part to the commercial EDA industry, which has provided the innovation and tools used throughout the design process, and the verification work that has become a specialty in its own right with dedicated conferences and standards.

The open-source ISA of RISC-V has generated a lot of interest around custom processor design options and the associated design freedoms beyond the roadmap of the mainstream processor IP providers. Thus, RISC V has enabled any SoC developer to consider designing a bespoke processor, which in turn has stimulated the interest in adapting the established SoC design verification (DV) flows based on UVM and SystemVerilog to also address the complexities of processor

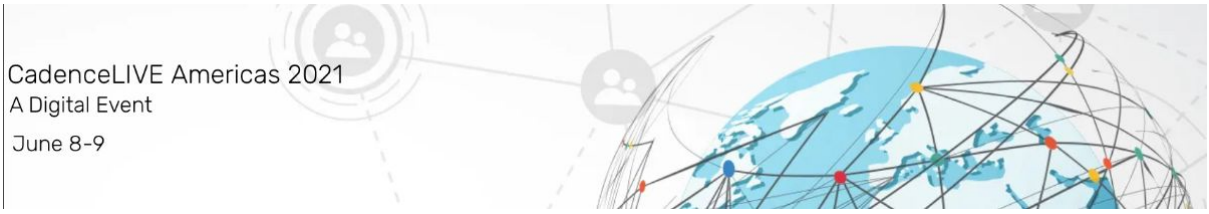
verification. On top of this, the open-source ISA of RISC-V has renewed the interest in open-source hardware IP. With this background, the OpenHW Group was formed to enable the community to collaboratively develop open-source hardware IP with industrial-strength verification, to provide the trust and confidence that is normally associated with commercial IP quality.

To read the full blog post by Steve Richmond (**Silicon Labs**), Mike Thompson (**OpenHW Group**), and Lee Moore (**Imperas**) on Semiconductor Engineering, [click here.]



Learn more

Events



Imperas at CadenceLIVE Americas, June 8-9, 2021

Imperas participating at the online virtual event highlighting the latest advances for UVM RISC-V Verification with RISC-V Processor Reference Models and SystemVerilog.

Two technical presentations on the latest advances for RISC-V verification:

'The Step-and-Compare methodology for high-quality RISC-V

processor verification’

‘The open verification method used by OpenHW for the CV32E40P RISC-V core’

During the live sessions and breaks, Imperas staff will be available for interactive Q&A with attendees throughout the event.

Discover more

Articles

ARTICLES FROM SEMICONDUCTOR ENGINEERING
DEEP INSIGHTS FOR THE TECH INDUSTRY

The Verification Mindset

What makes a good verification engineer? It’s not always about technical expertise, and it’s rarely just about verification. Ann Steffora Mutschler explains. Read more.

RISC-V Targets Data Centers

Open-source architecture is gaining some traction in more complex designs as ecosystem matures. Read the article by Ann Steffora Mutschler. Read more.

Merging Verification And Test

Reliability concerns throughout a device’s lifetime are driving fundamental changes in where and when these functions occur. Brian Bailey offers his insights. Read more.

Putting Limits On What AI Systems Can Do

Developing these systems is just part of the challenge. Making sure they only do what they're supposed to do maybe even harder. Article by Ed Sperling. Read more.

Release information

OVP and riscvOVPsim RELEASE NEWS

The latest Imperas and OVP release at the Open Virtual Platforms website.

For an introduction to RISC-V the free single core envelope model, called riscvOVPsim, is an excellent starting point, which can be configured for all the ratified ISA features and includes support of the draft specifications for Bit Manipulation and Vectors.

The latest version was uploaded on 26 February 2021, Version: 20210226.0 and is available via GitHub here.

The free enhanced riscvOVPsimPlus, including many more features including full configurable instruction trace, GDB/Eclipse debug, and memory configuration options, plus the RISC-V Vector and other test suites, is now available on the OVP website here.

riscvOVPsim, learn more