Imperas Newsletter – November 2021

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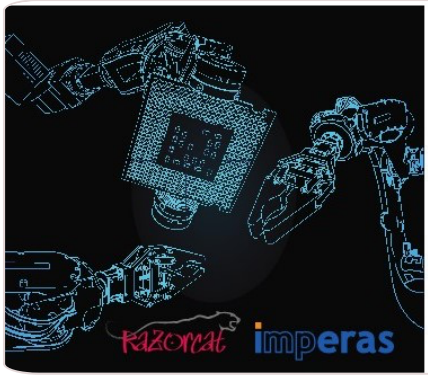
RISC-V Reference Model for Processor DV

Latest News



Imperas Models of Arm Processors now available in TESSY by Razorcat

"Palfinger is the global leader for innovative crane and lifting solutions," said **Hermann Haslauer, Head of Embedded Software Support Engineering at Palfinger Europe GmbH**. "As our embedded development teams develop and implement our roadmap for digitalization and artificial intelligence, the need for software quality testing has never been greater. The TESSY tool together with the Imperas virtual platform simulators and OVP models of Arm processors, are a quality combination that we use as a foundation of our software test and maintenance process."

Imperas simulation technology and reference models are now available within the TESSY environment for the automation of embedded software testing and regression management

For more information, please click here.

Events

58 DESIGN AUTOMATION CONFERENCE

FROM CHIPS TO SYSTEMS — LEARN TODAY, CREATE TOMORROW

Imperas at Design Automation Conference, December 5-9 2021

Imperas will be participating at DAC on the RISC-V Pavilion for in-person demonstrations and discussions with the Imperas team. Presentations will also be featured in both the DAC and RISC-V Summit technical conferences, which are co-located for 2021.

RISC-V processor verification methodology with dynamic testbench for asynchronous events
Speaker: **Man Wai (Manny) Wright – Imperas Software**
When: **Monday, December 6th, 5:00pm**
Where: **Designer, IP and Embedded Systems Track**

SoC Architectural Exploration for AI and ML accelerators with RISC-V
Speaker: **Simon Davidmann – Imperas Software**
When: **TBD**
Where: **Designer, IP and Embedded Systems Track**

For more information, or to schedule a demonstration session at DAC 2021, please contact the Imperas team via info@imperas.com.

Click here for more information about DAC 2021

Imperas at the RISC-V Summit, December 6-8 2021

As a proud Diamond sponsor of the 2021 RISC-V Summit, Imperas will be delivering keynote talks and presentations. In addition, an exhibition booth will feature demonstrations on the Imperas solutions for RISC-V simulation, including RISC-V processor verification and software development.

For more information, or to set up meetings with the Imperas team during the summit, please contact info@imperas.com.

Click here for more information about the RISC-V Summit 2021.

ARTICLES FROM SEMICONDUCTOR ENGINEERING
DEEP INSIGHTS FOR THE TECH INDUSTRY

Week In Review: Design, Low Power
FMEDA-driven verification; Arm virtual models for IoT; mmWave acquisition; TSMC N3/N4 certifications.

To read the full article by **Jesse Allen**, click here

What's Next For Emulation
Technologies must evolve to keep up with changing demands, and emulation is no exception.

To read the full article by **Brian Bailey**, click here.

High-Level Synthesis For RISC-V
Abstraction is the key to custom processor design and verification, but defining the right language and tool flow is a work in progress.

To read the full article by **Brian Bailey**, click here.

Release Information

riscvOVPsim and riscvOVPsimPlus - LATEST NEWS

The latest Imperas and OVP release at the Open Virtual Platforms website.

Open Virtual Platforms

For an introduction to RISC-V the free single-core envelope model, called

riscvOVPsim, is an excellent starting point, which can be configured for all the ratified ISA features and includes support of the draft specifications for Bit Manipulation and Vectors.

The latest version was is available via GitHub here.

The free enhanced **riscvOVPsimPlus**, including many more features including full configurable instruction trace, GDB/Eclipse debug, and memory configuration options, plus the RISC-V Vector and other test suites, is now available on the OVP website here.

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