Imperas Newsletter – Nov. 2022

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The leader in RISC-V simulation solutions

News

RISC-V® Summit

Imperas sponsor and contributor for the RISC-V Summit, December 12-15

Imperas is proud to be a contributing Diamond sponsor for this year's RISC-V Summit. Imperas will showcase solutions for RISC-V processor verification, custom instruction design flows, and software development, including a keynote on RISC-V Processor verification plus many other activities.

What: RISC-V Summit
Where: San Jose McEnery Convention Center
When: RISC-V International Members Meeting Day is on Dec. 12th
Conference and Exhibition Dec. 13th & 14th, Tutorials Dec. 15th

Keynote:
Improving RISC-V quality with verification standards and advanced methodologies
Speaker: Simon Davidmann, CEO, Imperas Software &
Verification Task Group Chair, OpenHW Group
When: Tuesday, December 13, 10:00am

Expo Presentation:
RISC-V Models for Verification, Software Development and Architectural

Exploration

Speaker: Larry Lapides, Imperas Software
When: Tuesday, December 13, 1:30pm

Conference Presentation:
The new verification ecosystem that supports RISC-V verification for all adopters
Speakers: Lee Moore, Imperas Software
Dave Kelf, CEO, Breker Verification Systems
When: Tuesday, December 13, 4:20pm

Expo Presentation:
Introduction to RISC-V Verification with the open standard RVVI (RISC-V Verification Interface)
Speaker: Aimee Sutton, Imperas Software
When: Wednesday, December 14, 1:40pm

Conference Presentation:
The continuum of RISC-V Compliance and Verification testing
Speakers: Simon Davidmann, CEO, Imperas Software
& Verification Task Group Chair, OpenHW Group
Allen Baum, Esperanto Technologies
& Chair of the RISC-V International Architecture Test SIG
When: Wednesday, December 14, 4:00pm

Tutorial:
Choosing appropriate verification techniques for desired RISC-V processor quality
Speakers: Lee Moore, Imperas Software
Aimee Sutton, Imperas Software
When: Thursday, December 15, 10:30am

Please stop by the **Imperas booth #D3** to see all the latest demonstrations of simulation and virtual platform technology for RISC-V based designs, including RISC-V processor Design Verification (DV) and architectural exploration with custom instruction, plus support for the latest RISC-V specifications for Vectors and Bit Manipulation.

For more information, or to set up meetings with the Imperas team at the RISC-V Summit 2022, please contact info@imperas.com.

Upcoming Events

Imperas will participate at RISC-V Days Tokyo 2022 Autumn, November 16th-18th

Imperas, together with local partner eSol Trinity, will provide insights and solutions for RISC-V processor verification and extensions with custom instructions, in conjunction with tools and solutions to accelerate embedded software development.
Stop by the Imperas booth and see all the latest demonstrations and virtual platform technology for RISC-V based designs, including verification and custom instruction, plus support for the latest RISC-V specifications for Vectors and Bit Manipulation.

RISC-V high quality verification with open standard RVVI and ImperasDV

RISC-V is extending the design freedoms for SoC developers with optimized processors. This talk outlines **RVVI** (RISC-V Verification Interface), an open standard interface for RISC-V processor verification with efficiency, reusability and flexibility. Highlights will cover examples of testing some popular open-source IP cores, and guidance for new processor DV projects.

Speaker: Shuzo Tanaka, eSOL TRINITY Co., Ltd.
Co-Author: Simon Davidmann, Imperas Software
Co-Author: Lee Moore, Imperas Software
Where: Pacifico Yokohama, Tokyo, Japan

For more information and registration, please visit RISC-V Days Tokyo 2022, or to set up meetings with Imperas, please contact info@imperas.com.

Imperas presents at New York City RISC-V Group Meeting, November 16

Imperas will present updates on the RISC-V Ecosystem that supports new design innovations with RISC-V via Flexibility With Compatibility. At this hybrid event, with an in-person element at The Cooper Union for the Advancement of Science and Art, speakers will describe their latest research and development involving RISC-V.

The RISC-V Ecosystem: Building In Flexibility With Compatibility
Traditional software ecosystems have developed around a common set of hardware configurations, but RISC-V offers unique flexibility. But will this flexibility lead to fragmentation and chaos? This presentation looks at the RISC-V ecosystem, both the successes and areas with work still required. Mass adoption is dependent on the efficiencies of scale that in turn depend on compatibility while supporting the value added-optimizations and differentiation. Has the RISC-V approach, based on ecosystem-first strategy, built in sufficient support for flexibility with compatibility?

Speaker: Larry Lapides, Imperas Software
When: Wednesday, November 16th, 5:45pm EST
Where: Hybrid event
The Cooper Union for the Advancement of Science and Art, NY

Free registration and more details are available at this link.

Imperas presents at the DVClub Europe event on RISC-V Verification Strategies on November 29th

RISC-V processor verification with new open standard RVVI based methodology

This talk outlines **RVVI** (RISC-V Verification Interface), an open standard interface for RISC-V verification including the integration methodology for the processor RTL (DuT) and reference model within a unified SystemVerilog testbench. It discusses a range of approaches based on the verification test plan needs for proof-of-concept test chips or research projects, to high-reliability application and high-volume silicon production. RVVI also addresses the complexity of the functional verification for superscalar, out-of-order, multi-hart, multi-thread, vector accelerators, privileged and debug modes of operation. Together these guidelines help to adapt the current industry standard SoC verification methods for RISC-V processor DV, and establish a common framework that supports reuse and shared contributions across the whole DV community.

Speaker: Simon Davidmann, Imperas Software Ltd
When: Tuesday, November 29th, 2022: 12pm to 1:30pm (GMT)
Where: Virtual event

This event is free to attend but registration is required, please visit DVClub to register.

Imperas at DVCon Europe, December 6th and 7th

Imperas will present together with Dolphin Design the latest advances for RISC-V Verification with RISC-V Processor Reference Models and Verification IP at DVCon Europe 2022

Case Study:

Development and Verification of RISC-V Based DSP Subsystem IP

To accelerate the development of software, a virtual platform (software simulation) flow is used. This starts with just a single processor model, the same OVP model used for DV, instantiated in a SystemC environment for basic bare metal software bring up. This paper will present the single processor DV and virtual platform methodologies and results, and discuss the extensions to these methodologies for DV and software development for the processing subsystem.

Co-author: Pascal Gouedo, Dolphin Design
Co-author: Damien Le Bars, Dolphin Design
Co-author: Olivier Montfort, Dolphin Design
Co-author: Lee Moore, Imperas Software
Co-author:: Aimee Sutton, Imperas Software
Co-author: Larry Lapides, Imperas Software
When: TBD

Please visit DVCon Europe, for more information.

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RISC-V International Members Meeting Day is on Dec. 12th

For more details, follow this link.

Articles

RISC-V Takes Embedded World 2022 by Storm

I love computers (but only in a manly-man way, you understand). I'm not talking about the end-products that sit on our desks, hang out in our pockets, or lurk around us as we meander our way through the world, although I'm certainly fond of these little rascals—I'm much more interested in their "brains" in the form of their processing units where all the decision-making and number-

crunching takes place...

To read the full **EE Journal** article by **Max Maxfield**, click here.

Toward Domain-Specific EDA. Is the tools market really changing, or has this always been the case?

One such change that is starting to find its way into the design methodology is shift from static tools to dynamic ones. A static tool will look at the design and optimize it independent of any particular use case or scenario. Dynamic optimization adds one or more scenarios that are used as input to the optimization process, allowing the tools to perform more focused optimizations. This started with power optimization when performing clock or power gating, which used to be a static operation. These techniques can be improved further by knowing exactly how and when parts of the design need to be active. This also is driving the resurgence of processor design where custom processors can be created that are optimal for specific tasks.

To read the full **Semiconductor Engineering** article by **Brian Bailey**, click here.

Verification Methodologies Evolve, But Slowly

Semiconductor Engineering sat down to discuss digital twins and what is required to develop and verify new chips across a variety of industries, such as automotive and aerospace, with Larry Lapides, vice president of sales for Imperas Software; Mike Thompson, director of engineering for the verification task group at OpenHW; Paul Graykowski, technical marketing manager for Arteris IP; Shantanu Ganguly, vice president of product marketing at Cadence; and Mark Olen, director of product management at Siemens EDA. What follows are excerpts of that conversation…

To read the full **Semiconductor Engineering** article by **Brian Bailey**, click here.

Part 1 of this discussion is here.

Part 2 of this discussion is here.

Foundational Changes In Chip Architectures

Technology often progresses in a linear fashion. Each step provides incremental improvement over what existed before, or to overcome some new challenge. Those challenges come from a new node, new physical effect, or limitation, etc. While this works very well, and many of the individual steps are brilliant, it is building on a house of cards in that if something at the base were to fundamentally change, the ripple effects throughout the design, implementation, and verification can be very significant…

To read the full **Semiconductor Engineering** article by **Brian Bailey**, click here.

Bespoke Silicon Rattles Chip Design Ecosystem

From specific design team skills, to organizational and economic impacts, the move to bespoke silicon is shaking things up. Bespoke silicon designers today are a rare breed, capable of understanding the unique requirements of a specific domain, as well as a growing array of issues that can crop up in multiple stages of the design flow. At the most basic level, they need to understand what works best in hardware, what works best in software, and how to tightly integrate both to optimize performance and power….

To read the full **Semiconductor Engineering** article by **Ann Steffora Mutschler**, click here.

Bug-Free Designs. Does anyone really care if a design is bug-free?

It is possible in theory to create a design with no bugs, but it's impractical, unnecessary, and extremely difficult to prove for bugs you care about. The problem is intractable because the potential state space is enormous for any practical design. The industry has devised ways to handle this complexity, but each has limitations, makes assumptions, and employs techniques that abstract the problem. Industry best practices are to try and identify bugs that cause problems and to fix those. Of the three primary techniques available, it is important to decide which is the best for each problem…

To read the full **Semiconductor Engineering** article by **Brian Bailey**, click here.

Chip Design Shifts As Fundamental Laws Run Out Of Steam
Dennard scaling is gone, Amdahl's Law is reaching its limit, and Moore's Law is becoming difficult and expensive to follow, particularly as power and performance benefits diminish. And while none of that has reduced opportunities for much faster, lower-power chips, it has significantly shifted the dynamics for their design and manufacturing...

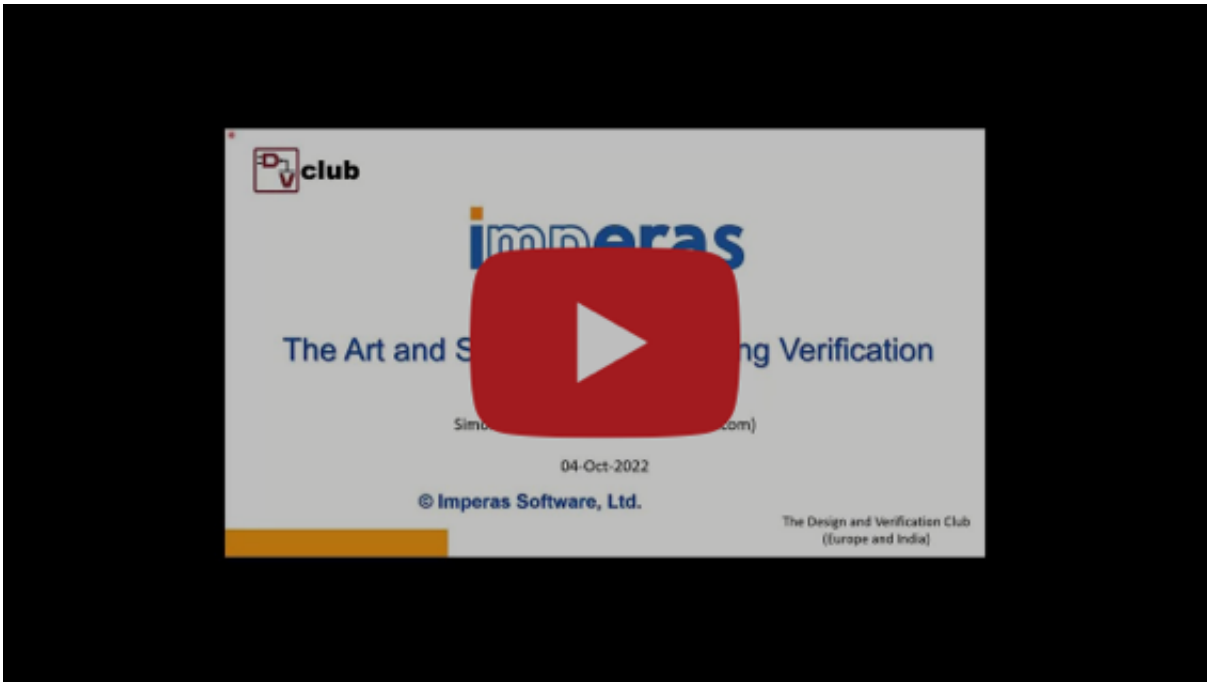
To read the full **Semiconductor Engineering** article by **Ann Steffora Mutschler**, click here.

Event Videos

OPENHW TV

Mike Thompson, Director of Engineering, Verification Task Group, OpenHW Group hosts a panel discussion with **Simon Davidmann**, Chair of OpenHW Verification Task Group and CEO at Imperas Software, **Peter**

Lewin, Director of CPU Ecosystems at Imagination Technologies, and **Rupert Baines**, Chief Marketing Officer at Codasip.

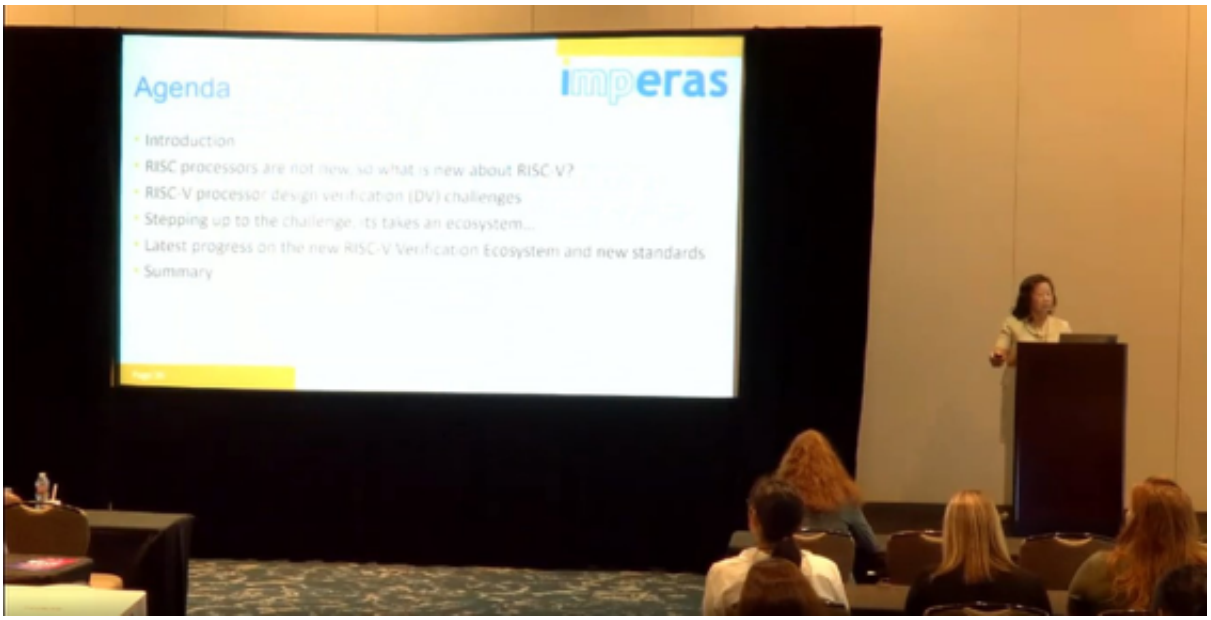


At the recent DVClub event on Automated Verification Checks, **Simon Davidmann** delivered a presentation entitled: **The art and science of automating verification checking**

You can also download the slides.

At the recent RISC-V Virtual Career Fair, **Larry Lapides** presented a few **good reasons for joining Imperas Software**.

At the recent SemIsrael Tech Webinar, **Larry Lapides** talked about advanced RISC-V processor verification. You can also download his slides here.



At the WISH (Women in Semiconductor Hardware) Conference, **Manny Wright** gave a presentation entitled: **Open-Source Has a Great Price, But Verification Adds the Real Value**. Click the above image - Manny's presentation starts at 22 minutes.

Release Information

riscvOVPsim and riscvOVPsimPlus - LATEST NEWS

The latest Imperas and OVP release at the Open Virtual Platforms website.

For an introduction to RISC-V the free single-core envelope model, called **riscvOVPsim**, is an excellent starting point, which can be configured for all the ratified ISA features and includes support of the latest ratified specifications including Bit Manipulation, Crypto (scalar) and Vectors.

The latest version is available via GitHub here.

The free enhanced **riscvOVPsimPlus**, including many more features including full configurable instruction trace, GDB/Eclipse debug, and memory configuration options, plus the RISC-V Vector and other test suites, is now available on the OVPworld website here.

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