Imperas Newsletter – October 2021

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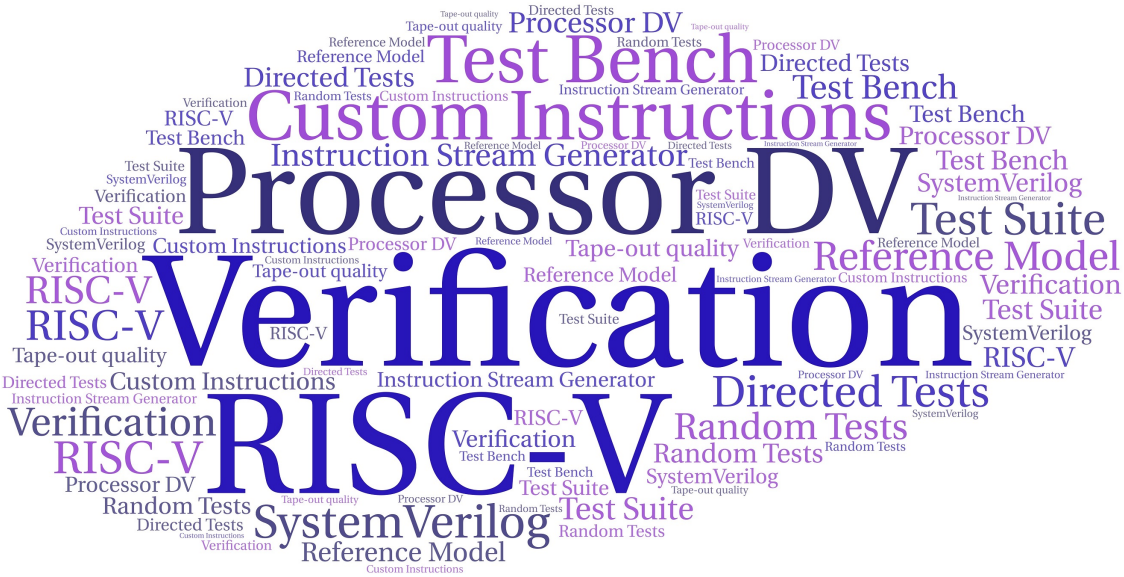
RISC-V Reference Model for Processor DV

Feature Article



RISC-V International: Developing standards-based verification environments for extensible RISC-V processor cores

By Kevin McDermott, Imperas Software

The open ISA of RISC-V means any SoC developer can now design a custom processor - moving the verification task from a few specialist suppliers to all SoC developers. This article looks at the industrial-grade verification and open methodology as used by the OpenHW verification working group.

To read the full article published by **RISC-V International**, please click here.

ARTICLES FROM  SEMICONDUCTOR ENGINEERING
DEEP INSIGHTS FOR THE TECH INDUSTRY

Software-Hardware Co-Design Becomes Real

Automatic mapping of software onto existing hardware, or using software to drive hardware design, are highly desired but very difficult.

To read the full article by **Brian Bailey**, click here.

Optimization Driving Changes In Microarchitectures

New approaches emerge as demand for improved power and performance overwhelm design tools.

To read the full article by **Ann Steffora Mutschler**, click here.

Containing The Explosion In Data

Designs are getting bigger, verification runs longer, and every stage of development and deployment provides valuable data — if you can find it.

To read the full article by **Brian Bailey**, click here.

Tradeoffs Between Edge Vs. Cloud

As localized processors become more powerful, what works best where?

To read the full article by **Brian Bailey**, click here.

Events

Boston Area RISC-V Group
Tue, Oct 5th 2021 - 6:00 PM (EDT)
Virtual Event

Imperas and Andes Technology are co-hosting the next RISC-V Boston Group Meeting on **Optimizing a RISC-V processor with Vector Extensions for AI applications**.

During the virtual event, **John Min, Andes Technology** will talk about *Memory Bandwidth: The Real Challenge for RISC-V Vector Processors*. **Katherine (Kat) Hsu, Imperas** will focus on *Software development: The Critical Path for AI SoC*. And, as the guest speaker, **Dave Baker, VP Digital Design, Luminous Computing** will share *Comments on Experiences with RISC-V ISA*.

Registration for the event is free. For more details, please click here.

September's RISC-V Forum, which covered the latest trends and developments in hardware Design Verification of RISC-V Vector Extensions and software development for Machine Learning applications is now available on-demand. During the Forum, Imperas presented two papers:

Software Development for ML and RISC-V Vector Accelerators
Co-author/Speaker: **Simon Davidmann, Imperas Software**
Co-author: **Lee Moore, Imperas Software**

Click here for immediate access to the slides and video.

Design Verification with Step-and-Compare for RISC-V Vector Extensions
Co-author/Speaker: **Lee Moore, Imperas Software**

Co-author: **Simon Davidmann, Imperas Software**

Click here for immediate access to the slides and video.

Save the Date

Remember to put a note in your diaries for this year's RISC-V Summit and Design Automation Conference, which will be co-located at San Francisco's Moscone Center.

Please click on these links to register for each:
RISC-V Summit 2021
DAC 2021

Release Information

riscvOVPsim and riscvOVPsimPlus - LATEST NEWS

The latest Imperas and OVP release at the Open Virtual Platforms website.

For an introduction to RISC-V the free single-core envelope model, called **riscvOVPsim**, is an excellent starting point, which can be configured for all the ratified ISA features and includes support of the draft specifications for Bit Manipulation and Vectors.

The latest version was is available via GitHub here.

The free enhanced **riscvOVPsimPlus**, including many more features including full configurable instruction trace, GDB/Eclipse debug, and memory configuration options, plus the RISC-V Vector and other test suites, is now available on the OVP website here.

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