Imperas Newsletter – Oct. 2022

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News

Simon Davidmann new Chair of the OpenHW Verification Task Group

Simon Davidmann has been appointed as Chair of the OpenHW Verification Task Group (VTG) with an expanded charter to drive the developing verification infrastructure and methodologies applicable to all RISC-V adopters.

For more details on the new plan, please register for the OpenHW TV event on October 27th.

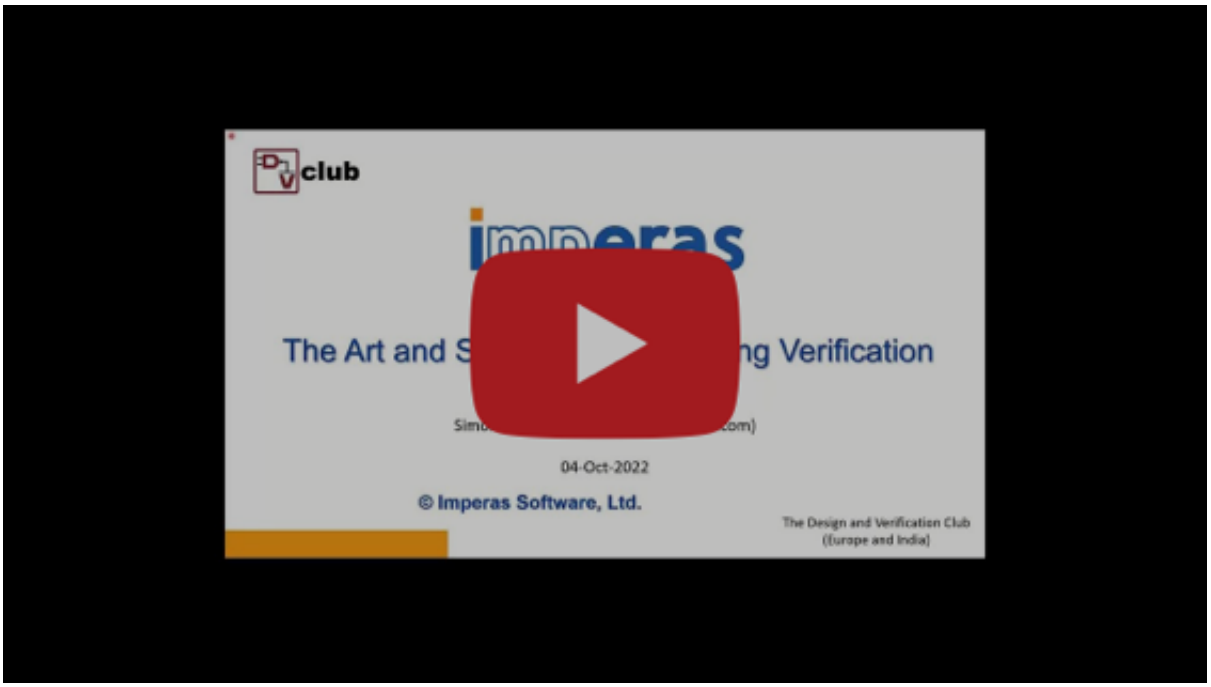
Upcoming Events

Imperas recently presented at the virtual DVClub event on Automated Verification Checks on October 4th, 2022.

The art and science of automating verification checking

As with many aspects of modern verification plans, the methodologies and techniques are revised and improved over time to improve efficiency and quality. Specifications are the reference for all the key requirements from communication protocols, bus standards, and processor ISAs so these are the essential starting point. Automation starts with the specifications and supports the development of generators for coverage libraries, score boarding, event sequences, and test suites. Using examples from actual projects, this talk highlights the latest software generators for automating coverage tests.

Speaker: Simon Davidmann, Imperas Software
Where: Virtual event



If you missed the live session, PDFs of the slides are now available.

Imperas will present at Andes RISC-V Con 2022 in Silicon Valley on October 18th, 2022

When: Tuesday, October 18th, 2022: 10am to 6pm (PDT)
Where: DoubleTree by Hilton Hotel, San Jose, California

Architectural exploration for RISC-V optimized domain-specific processors with Imperas and Andes ACE
This talk will outline the architectural exploration process to optimize Andes ACE extensions for your applications using the Imperas reference models and analysis tools.
Speaker: Manny Wright, Imperas Software

In addition to the talk with Manny, we will also participate in a panel discussion:

RISC-V Ecosystem panel: From Edge to Cloud
Moderator: Daniel Nenni, Founder, SemiWiki
Panelists: Andes, Crypto Quantique, Green Hills Software, IAR Systems, Imperas Software

This event is free to attend but registration is required, please visit Andes RISC-V Con to register.

For more information, or to set up meetings with Imperas at Andes RISC-V Con, please email info@imperas.com

Imperas on OpenHW TV on October 27, 2022

The OpenHW Group welcomes **Simon Davidmann of Imperas Software**, a founding member of OpenHW, as the new Chair of the OpenHW Verification Task Group (VTG). As part of the CORE-V roadmap, the VTG is updating the successful CORE-VERIF framework to address both the increasing design complexity and improve the DV efficiency for the anticipated bandwidth required for all the new CORE-V cores in development.

To address the dual goals of improving and enhancing the OpenHW internal flows for the CORE-V roadmap and help lead the industry adoption of RISC-V, and the associated verification workload, the VTG has started a new methodology project. This episode highlights the new OpenHW VTG Advanced RISC-V Verification Methodology (ARVM) project and outlines the initial concepts and plans for a couple of the sub-projects:

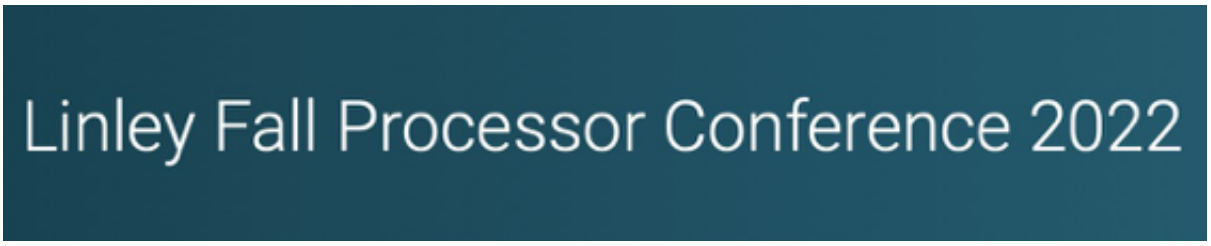
- **ARVM - Functional Coverage:** developing open-source VIPs that can be used for many different core configurations/implementations
- **ARVM - Standards**: defining and implementing evolving interface standards (such as RVVI) for test bench components to enable better test bench component reuse and potentially stimulate the availability of compatible VIPs

OpenHW TV – Episode S03/E08: Advancing RISC-V Processor Verification
Speakers: Simon Davidmann, Chair of OpenHW VTG & CEO, Imperas Software
Guest speakers TBA
When: Thursday, October 27th, 2022: 4pm (London) / 8am (San Jose, CA)
Where: Virtual online event

Following the updates and presentations, all the panelists will be available for

the live Q&A session with audience participation.

Registration is now open at this link.



Linley Fall Processor Conference 2022

The Imperas team will be in attendance throughout the conference and available
for 1-1 meetings and discussions on RISC-V functional verification and virtual prototypes for software development.

Where: Hyatt Regency Hotel, Santa Clara, CA
When: November 1-2, 2022

This is a hybrid event, register at this link. To set up a 1-1 meeting, contact us via info@imperas.com

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Imperas will participate at RISC-V Days Tokyo 2022 Autumn, November 16th-18th, 2022

Imperas, together with local partner eSol Trinity, will provide insights and solutions for RISC-V processor verification and extensions with custom instructions, in conjunction with tools and solutions to accelerate embedded software development.
Stop by the Imperas booth and see all the latest demonstrations and virtual

platform technology for RISC-V based designs, including verification and custom instruction, plus support for the latest RISC-V specifications for Vectors and Bit Manipulation.

RISC-V high quality verification with open standard RVVI and ImperasDV
RISC-V is extending the design freedoms for SoC developers with optimized processors. This talk outlines **RVVI** (RISC-V Verification Interface), an open standard interface for RISC-V processor verification with efficiency, reusability and flexibility. Highlights will cover examples of testing some popular open-source IP cores, and guidance for new processor DV projects.

Speaker: Shuzo Tanaka, eSOL TRINITY Co., Ltd.
Co-Author: Simon Davidmann, Imperas Software
Co-Author: Lee Moore, Imperas Software
Where: Pacifico Yokohama, Tokyo, Japan

For more information, or to set up meetings with Imperas, please contact info@imperas.com.

Imperas will present at the DVClub Europe event on RISC-V Verification Strategies on November 29th, 2022

RISC-V processor verification with new open standard RVVI based methodology
This talk outlines **RVVI** (RISC-V Verification Interface), an open standard interface for RISC-V verification including the integration methodology for the processor RTL (DuT) and reference model within a unified SystemVerilog testbench. It discusses a range of approaches based on the verification test plan needs for proof-of-concept test chips or research projects, to high-reliability application and high-volume silicon production. RVVI also addresses the complexity of the functional verification for superscalar, out-of-order, multi-hart, multi-thread, vector accelerators, privileged and debug modes of operation. Together these guidelines help to adapt the current industry standard SoC verification methods for RISC-V processor DV, and establish a common

framework that supports reuse and shared contributions across the whole DV community.

Speaker: Simon Davidmann, Imperas Software Ltd
When: Tuesday, November 29th, 2022: 12pm to 1:30pm (GMT)
Where: Virtual event

This event is free to attend but registration is required, please visit DVClub to register.

Imperas presents together with Dolphin Design the latest advances for RISC-V Verification with RISC-V Processor Reference Models and Verification IP at DVCon Europe 2022

Development and Verification of RISC-V Based DSP Subsystem IP: Case Study

The RISC-V ISA has been gaining momentum in the semiconductor community because of the design freedoms of the open specification. To date, the focus in the community has been on the development and verification of individual domain-specific processors and the software that runs on them. One of the use cases for those domain-specific processors is the instancing of multiple processors to create processing subsystems for AI/ML, audio processing and

general-purpose digital signal processing. This subsystem level of processor integration poses new challenges for both hardware and software, not only with the individual RISC-V processors but also at the subsystem level.
New challenges faced include the verification of custom features in the processors, development of the communication fabric for the multiple processors and software development on the processor subsystem. There are also some existing challenges, specifically the verification of the base RISC-V processor.
To accelerate the development of software, a virtual platform (software simulation) flow is used. This starts with just a single processor model, the same OVP model used for DV, instantiated in a SystemC environment for basic bare metal software bring up.
This paper will present the single processor DV and virtual platform methodologies and results, and discuss the extensions to these methodologies for DV and software development for the processing subsystem.

Co-author: Pascal Gouedo – Dolphin Design
Co-author: Damien Le Bars – Dolphin Design
Co-author: Olivier Montfort – Dolphin Design
Co-author: Lee Moore – Imperas Software
Co-author:: Aimee Sutton – Imperas Software
Co-author: LarryLapides – Imperas Software
When: TBD

For more information on DVCon Europe please visit https://dvcon-europe.org

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Articles

EDN

Four things to know about the Intel Pathfinder for RISC-V

As if Intel testing the RISC-V waters wasn't news in itself, the semiconductor behemoth's Intel Pathfinder for RISC-V initiative is now making the headlines. RISC-V is an open standard instruction set architecture (ISA) that offers chip developers the freedom to configure a custom processor with standard extensions and configuration options.

Vijay Krishnan, general manager of RISC-V Ventures at Intel, acknowledges that the adoption of RISC-V is at an inflection point across multiple markets and applications. Intel, which spearheads the x86 ISA world, has been proactive in the RISC-V space for quite some time. Now, its Pathfinder platform is promising to bolster the RISC-V design ecosystem for developing and prototyping chip designs with robust software and industry-standard toolchains…

To read the full **EDN** article by **Majeed Ahmad**, click here.

A Reborn Intel Enters the RISC-V Ecosystem

For the world's largest CPU vendor to become a genuine facilitator for the open [standard] RISC-V community, Intel must demonstrate its intent and commitment. Is its Pathfinder initiative for RISC-V enough? Can Intel gain the trust from those in the RISC-V ecosystem? At stake is the future of Intel Foundry Services….

To read the full **Ojo-Yoshida Report** article by **Junko Yoshida**, click here.

E&T: Intel leans harder on RISC-V

Much like IBM after the PC architecture ran away from it and almost collapsed Big Blue's highly profitable minicomputer and mainframe businesses, Intel has

been through some soul-searching in the wake of Arm's expansion from the world of cellular phones into just about everything else.
Intel has moved from a company that sued relentlessly to try to maintain control of the instruction set architecture (ISA) that powered the PCs that crippled IBM's original business to one that now sees or at least claims to see the advantages in an [open standard] ISA that anyone can use to build their own processors. Intel is now one of RISC-V's biggest fans, launching this week a programme to try to get more chip designers onboard with the architecture….

To read the full **Engineering & Technology** article by **Chris Edwards**, click here.

ElectronicDesign 70 YEARS

Engineering Academy Tackles RISC-V in Next Educational Event Installment

The open [standard] RISC-V instruction set architecture (ISA) has taken the development community by storm as more companies have implemented chips based on RISC-V. The architecture is empowering a generation of developers by giving everyone, regardless of size, an opportunity to compete. It's also fostered a level of customization that's driving innovations in areas from microcontrollers to artificial intelligence.
As part of its new Engineering Academy educational platform, Electronic Design's September 8 event on Expanding the RISC-V Ecosystem will delve into RISC-V from multiple perspectives. Each session, led by industry leaders and subject matter experts, will cover topics ranging from chip and architecture designs through software development….

To read the full **Electronic Design** article by **William G. Wong**, click here.

ARTICLES FROM SEMICONDUCTOR ENGINEERING
DEEP INSIGHTS FOR THE TECH INDUSTRY

How Mature Are Verification Methodologies?

Semiconductor Engineering sat down to discuss differences between hardware and software verification and changes and challenges facing the chip industry, with Larry Lapides, vice president of sales for Imperas Software; Mike Thompson, director of engineering for the verification task group at OpenHW; Paul Graykowski, technical marketing manager for Arteris IP; Shantanu Ganguly, vice president of product marketing at Cadence; and Mark Olen, director of product management at Siemens EDA. What follows are excerpts of that conversation…

To read the full **Semiconductor Engineering** article by **Brian Bailey**, click here.

Part 1 of this discussion is here.

Verification Scorecard: How Well Is The Industry Doing?

Semiconductor Engineering sat down to discuss how well verification tools and methodologies have been keeping up with demand, with Larry Lapides, vice president of sales for Imperas Software; Mike Thompson, director of engineering for the verification task group at OpenHW; Paul Graykowski, technical marketing manager for Arteris IP; Shantanu Ganguly, vice president of product marketing at Cadence; and Mark Olen, director of product management at Siemens EDA. What follows are excerpts of that conversation…

To read the full **Semiconductor Engineering** article by **Brian Bailey**, click here.

Part 2 of this discussion is here.

Release Information

riscvOVPsim and riscvOVPsimPlus - LATEST NEWS

The latest Imperas and OVP release at the Open Virtual Platforms website.

For an introduction to RISC-V the free single-core envelope model, called **riscvOVPsim**, is an excellent starting point, which can be configured for all the ratified ISA features and includes support of the latest ratified specifications including Bit Manipulation, Crypto (scalar) and Vectors.

The latest version is available via GitHub here.

The free enhanced **riscvOVPsimPlus**, including many more features including full configurable instruction trace, GDB/Eclipse debug, and memory configuration options, plus the RISC-V Vector and other test suites, is now available on the OVPworld website here.

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