Imperas Newsletter – September 2021

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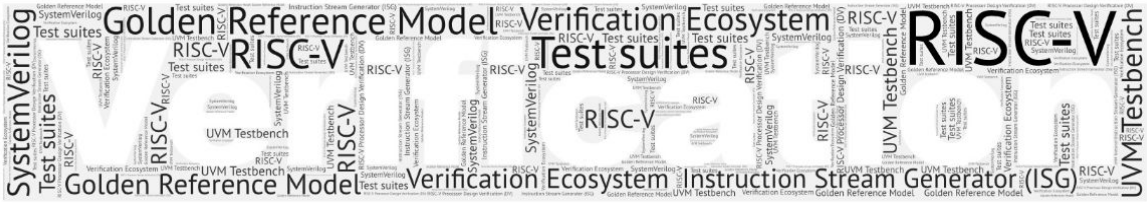
RISC-V Reference Model for Processor DV

Latest News



Over the past 12 months, we have had the honor in announcing a wide range of customers and partners using Imperas reference models including: Andes, IAR Systems, NSITEXE, NVIDIA Networking (Mellanox), OpenHW Group, RISC-V International, Seagate Technology, SiFive, Silicon Labs, and Valtrix Systems. With many more engaged in active projects, but they are yet to be publicly disclosed.

New Podcast

Well, technically… the compute power used by AI is increasing exponentially

Imperas Software's Senior Account Manager Katherine (Kat) Hsu discusses with **Catherine Sbeglia, Technology Editor for RCR Wireless News**, the biggest trends in the semiconductor industry, why consumers should care about AI processors and the technical challenges that open standard RISC-V helps solve.

To listen to the podcast, which is published on **RCR Wireless News**, click here.

New Article

Enabling industrial-grade open verification for RISC-V

The open nature of the RISC-V ISA means anyone can design a custom processor, moving the verification task from a few specialist suppliers to all SoC developers. In this article, **Kevin McDermott, vice president of marketing at Imperas Software**, looks at using industrial-grade verification and an open methodology to support verification of an open-source CV32E40P IP core.
To read the article published on **embedded.com** in full, click here.

Events

Imperas is participating in the online virtual event highlighting hardware Design Verification of RISC-V Vector Extensions and software development for Machine Learning applications on September 15, 2021.

To support hardware implementations Imperas will present the latest advances in the verification of RISC-V processors and Vector Extensions, and for software developers the use of virtual platforms to shift-left the key project schedules.

Software Development for ML and RISC-V Vector Accelerators
Co-author: **Simon Davidmann, Imperas Software**
Co-author: **Lee Moore, Imperas Software**
When: **September 15th 2021 at 8:35am PDT**

Design Verification with Step-and-Compare for RISC-V Vector Extensions
Co-author: **Lee Moore, Imperas Software**
Co-author: **Simon Davidmann, Imperas Software**

When: **September 15th 2021 at 9:15am PDT**

To register for the event, click here.

Imperas and Andes co-hosted the RISC-V Austin Group Meeting on optimizing a RISC-V processor with Vector Extensions for AI applications. Entitled 'The Real Challenge for RISC-V Vector Processors' there were talks by Andes and Imperas. Guest speaker **Dave Baker, VP Digital Design at Luminous Computing** also shared his comments on experiences with RISC-V ISA.

Software Development for AI SoCs

Speaker: **Katherine (Kat) Hsu, Imperas Software**

Now available on-demand, this talk discusses the different tasks of software development for AI SoCs, and explains how a virtual platform enables the “shift left” of schedules, many months before an FPGA prototype or hardware emulator is available.

To watch all the talks that were delivered during the meeting, click here.

This RISC-V Forum online event covered the latest trends and developments for Embedded Technology, which is the heart of RISC-V due to its flexible and adaptable architecture. During the Forum, Imperas presented an update and overview on the Free ISS (Instruction Set Simulator) for the OpenHW CORE-V IP Roadmap.

Getting started with the *Free* ISS for the OpenHW CORE-V IP Roadmap
Speaker: **Katherine (Kat) Hsu, Imperas Software**

To watch Kat's talk on-demand, click here.

ARTICLES FROM SEMICONDUCTOR ENGINEERING
DEEP INSIGHTS FOR THE TECH INDUSTRY

Designing Chips In A 'Lawless' Industry
Mind-boggling number of options emerge, but which is best often isn't clear.

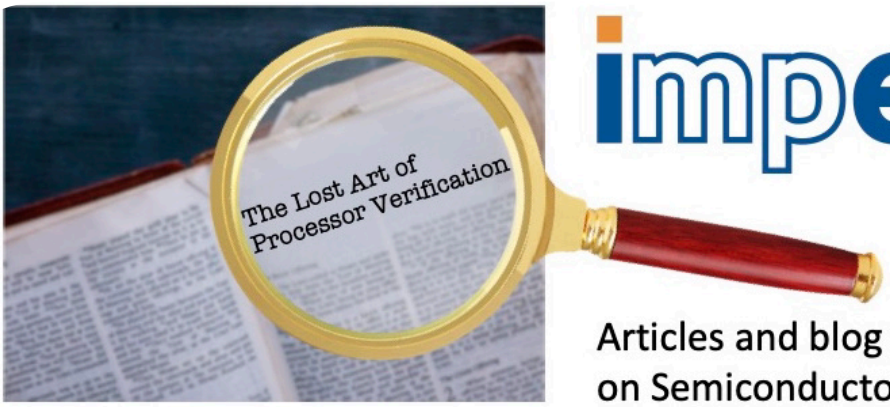
To read the full article by **Ed Sperling**, click here.

Continuous Education For Engineers
Companies that invest in their employees' education often get rewarded with more productive and happier workers.

To read the full article by **Brian Bailey**, click here.

Sweeping Changes Ahead For Systems Design
Demand for faster processing with increasingly diverse applications is prompting very different compute models.

To read the full article by **Ann Steffora Mutschler**, click here.



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Articles and blog posts featured on Semiconductor Engineering

RISC-V:
The 5 levels of simulation-based processor hardware design verification
RISC-V is enabling processor design freedoms to the broad community of SoC developers, but this also represents a migration of the processor design verification task from the teams at a few mainstream IP providers to all RISC-V adopters. Developers that accept the design freedoms of RISC-V must also undertake the appropriate level of verification responsibility.
In some cases, a simple comparison-based trace analysis is sufficient to confirm some level of basic operation of the processor, while designs targeted at volume production and/or high-reliability applications will justify significant additional verification efforts. The challenge of RISC-V is not just the verification task, but the correct selection of the quality level appropriate for the end application.

To read the article in full, click here.

Release Information

OVP and riscvOVPsim RELEASE NEWS

The latest Imperas and OVP release at the Open Virtual Platforms website.

OVP
Open Virtual Platforms

For an introduction to RISC-V the free single-core envelope model, called **riscvOVPsim**, is an excellent starting point, which can be configured for all the ratified ISA features and includes support of the draft specifications for Bit Manipulation and Vectors.

The latest version was is available via GitHub here.

The free enhanced **riscvOVPsimPlus**, including many more features including full configurable instruction trace, GDB/Eclipse debug, and memory configuration options, plus the RISC-V Vector and other test suites, is now available on the OVPworld website here.

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