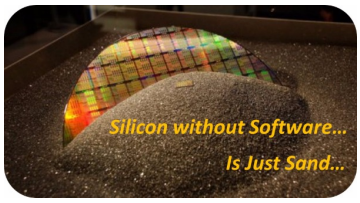
Revolutionizing Embedded Software Development

Imperas Newsletter: January 2019

"Silicon without software is just sand."



EVENTS

Imperas at the Embedded World Exhibition & Conference 2019

- **When**: February 26 - 28, 2019.
- **Where**: Nuremberg Exhibition Centre, Nuremberg, Germany.

You can use discount code B401530, courtesy of Imperas, to pre-register and receive a 3-day entrance e-ticket. Click this link.

Imperas will demonstrate virtual platform solutions for RISC-V compliance including extensions with custom instructions, in conjunction with tools to accelerate embedded software development and test.

- Visit Imperas on the RISC-V Foundation booth at Hall 3A-536.

Embedded World will also feature a dedicated RISC-V track with two papers by Imperas, on February 26, 2019:

- **"Methodology for Implementation of Custom Instructions in the RISC-V Architecture."**
- **"Compliance Methodology and Initial Results for RISC-V ISA Implementations."**

Read more here.

For more information, or to set up meetings with Imperas at Embedded World, please email info@imperas.com.

About Embedded World 2019

- View the complete Embedded World program.
- See www.embedded-world.de/en for event details.

Imperas is organizing a panel at the 2019 Design and Verification Conference & Exhibition (DVCon)

- **When**: February 25-28, 2019.
- **Where**: DoubleTree Hotel, San Jose, California, USA

"Verification and Compliance in the era of open ISA – Is the Industry ready to Address the Coming Tsunami of Innovation?" with Simon Davidmann, CEO of Imperas.

- **When**: February 27, 8:30am – 9:30am
- **Where**: Oak/Fir Room.

Read more here.

We hope to see you there! Please email info@imperas.com to meet with Imperas on virtual platforms for embedded software and systems development, debug and test, at DVCon!

About DVCon 2019

- For more information see https://dvcon.org

NEWS

SEMICONDUCTOR ENGINEERING

"IoT Device Security Makes Slow Progress"

New article in Semiconductor Engineering by Ann Steffora Mutschler, with Kevin McDermott.

Read it here.

OVP RELEASE NEWS

OVP: Fast Simulation, Free open source models, Public APIs: Open Virtual Platforms.

A new Imperas and OVP release became available November 2018. The releases included many enhancements to different CPU models.

For the Arm models we updated our variants for the Cortex-M7 and Cortex-M7F and restructured the model sources to simplify the maintenance of the different model families. We also added several new parameters to allow control over the implementation of different specified 'unpredictable' behaviors and also updated many disassembly and warning messages.

Our RISC-V envelope model as used in the RISC-V Foundation's Compliance Working Group had many improvements to take into account the evolving RISC-V specifications.

For MIPS, there were several enhancements for the I6500 and MIPSr5 models.

The OVP APIs were enhanced with many new functions for vector instructions for Arm and RISC-V processors.

The simulator core was enhanced to improve behavior and the license server was upgraded to support network device naming.

The Open Virtual Platforms portal is one of the most exciting open source software developments in the embedded software world since GNU created GDB.

- For embedded software developers, virtual platforms are increasingly important, especially for multi-core designs.

The resources on this portal can significantly accelerate your development and test.
