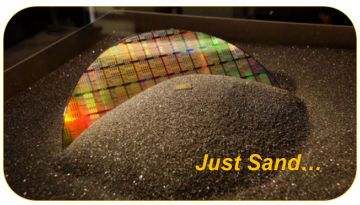
imperas

Revolutionizing Embedded Software Development

Imperas Newsletter: May 2016

"Silicon without software is just sand."

Updating you on what's new in the embedded software revolution.



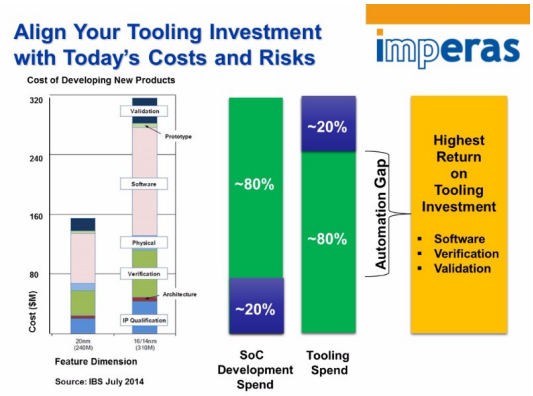
Viewpoint: Simon Davidmann, CEO Imperas

Looking ahead to DAC and Embedded TechCon in June in Austin.
Imperas will be in the Embedded Pavilion, booth #839.
Please contact us at sales@imperas.com to set up a meeting or demo.
We hope to see you there!

Please **follow us** on Linked In, and twitter **@ImperasSoftware**

Align Your Tooling Investment with Today's Development Costs and Risks

By Simon Davidmann



Economic decision makers need to look at ROI and the automation gap; aligning tooling investments with today's costs and risks in developing new products. IBS reports that as feature dimensions decrease one process node, development costs are now doubling! From about $160M at 20nm to $320M at 14/16nm.

Looking closer at the costs of developing new products, we see that of the total SoC development spend, over 80% is in verification, software and validation. Less than 20% of costs and risk is in IP qualification and physical layout aspects.

However, the average spend for tooling is an incongruous 20% / 80% reversed! Only 20% is spent on tools to solve 80% of the development risk. This is the **Automation Gap**.

Rationally addressing the percentage of costs of development / risk vs investment, the answer is clear: the highest return on tooling investment is in 3 areas: 1. Software 2. Verification and 3. Validation.
These are the areas Imperas virtual platforms were developed to address.
For more information, click here.

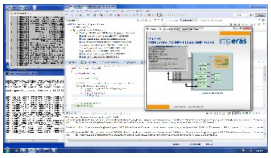
See You at DAC and Embedded TechCon 2016 in Austin, Texas!

Imperas will be showing our latest models and virtual platform solutions at DAC 2016, including embedded software and hardware development, debug and test applications.

- Join us on June 5-9 at the Austin Convention Center.
- The Imperas booth is located in the Embedded Pavilion, booth #839.

Read more here.

DAC Demo Highlights:



See Imperas virtual platform-based solutions for embedded software development, debug, analysis and verification.

- Imperas demos will show a variety of Open Virtual Platforms (OVP) models and virtual prototypes including processor models of ARM (including Cortex-A, R and M families) and Imagination Technologies (MIPS).

DAC Tutorial:

Imperas will deliver a tutorial on "Linux Porting and Bring Up, and Driver Development" featuring virtual platforms, as part of the System Software topic in the DAC Embedded Systems track.

- Monday, June 6, 2016, 10:30am - 12:00pm
- Location: 13AB

Embedded TechCon Presentations:

Pre-Silicon OS Porting, Bring Up and Driver Development

- Tuesday, June 7, 2016, 2:00-2:25pm
- Location: 13AB

Accelerating ARM Software Development, Debug and Test

- Tuesday, June 7, 2016, 2:30-2:55pm
- Location: 13AB

The Latest News and Roundup Articles

---

prpl Foundation Security Group Address IoT Security Challenges via Multi-Domain Virtualization

Article by Simon Davidmann in the first edition of new "prpl Perspectives" newsletter from the prpl Foundation.
Read more here.

ESL Flow is Dead?

New article by Brian Bailey with Simon Davidmann. Expecting the future to replicate the past always leads to surprises and when it comes to migration of abstraction for semiconductor design, the future remains unclear.
Read more here.

Automating System Design

Semiconductor Engineering article by Ann Steffora Mutschler, with Simon Davidmann.
Read more here.

System-Level Verification Tackles New Role

Roundup article by Brian Bailey in System Level Design, with Larry Lapides.
Read more here.

Automotive Virtual Platform Case Study: Audi

Audi
Case Study

For Audi (NIRA Dynamics) in automotive, software testing is mission-critical. Because failsafe quality is key, they needed an exhaustive testing solution, a high-level approach to verification of hardware/ software systems, with complete observability, controllability, and repeatability: Imperas virtual platforms.

With Imperas, engineers successfully ran months of road test data they had collected as stimuli, for comprehensive software test and analysis and to debug software, memory operation, and multiple ABS processor designs. Thousands of tests using this data ran nightly in regression suites. Advanced memory analysis ensured correct stack and heap behavior, with non-intrusive memory analysis to ensure that simulation results were valid. Overall, both bugs in the code, and also in some compilers used, were identified and fixed.
Read more here.

OVPsim Release News

imperas
OVP
Open Virtual Platforms

A new Imperas and OVP release is available, 20160323.0 (March 2016). New in this release are the OP API for building virtual platforms, the model of the ARM Cortex-A72 processor, and the addition of the iGen productivity tool for peripheral and platform building to OVPsim. The OP API provides flexibility and efficiency for complex platforms, including those with hierarchy. Transitioning to OP is seamless if iGen was used to build the platform.

The Open Virtual Platforms portal is one of the most exciting open source software developments in the embedded software world since GNU created GDB.

- For embedded software developers, virtual platforms are increasingly important, especially for multi-core designs.

The resources on this portal can significantly accelerate your development and test. The next release of OVPsim is expected to be available in June 2016.

Website LinkedIn Email Twitter