imperas

Revolutionizing Embedded Software Development

Imperas Newsletter: November 2016

"Silicon without software is just sand."

Updating you on what's new in the embedded software revolution.

Silicon without Software...
Just Sand...

Viewpoint: Simon Davidmann, CEO Imperas

ARM TechCon, in October was an excellent event; and we were honored to have been on Embedded Computing's Top Things to See at ARM TechCon list.

- If you missed the show, you can still view our technical presentation "Integrating Power Models into Instruction Accurate Virtual Platforms" here.
- We recently enhanced our website: see videos and demos here.

Imperas will also attend the embedded world conference, March 14-16, 2017 at the Exhibition Centre in Nürnberg, Germany. Imperas will be featuring two papers:

- "Using Virtual Prototypes to Improve the Traceability of Critical Embedded Systems"
- "Fast Fault Injection to Evaluate Multicore Systems Soft Error Reliability"

For more information about ARM TechCon highlights and demos, or to set up a meeting at embedded world, please email us at sales@imperas.com.

Please **follow us**: on Linked In, and twitter @ImperasSoftware

News from Imperas!
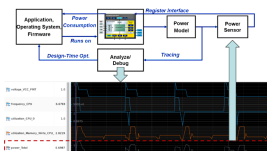
Integrating Power Models into Instruction Accurate Virtual Platforms for ARM-based MPSoCs

Imperas and OFFIS Technical Session at ARM TechCon

"Integrating Power Models into Instruction Accurate Virtual Platforms for ARM-based MPSoCs" by Imperas and OFFIS (Institute for Information Technology.) In embedded systems, extra-functional requirements like power consumption have been increasing in importance. For a power extension of an instruction accurate virtual platform: we equip an OVP Xilinx Zynq virtual platform with a dynamic voltage and frequency scaling (DVFS) compatible power model. Software on the virtual platform accesses the actual power consumption and performs power management through DVFS.

View it here.

Imperas and T&VS Partner to Update Software Verification and Validation Methodology for Embedded Systems

Imperas Software and Test and Verification Solutions (T&VS) partner to promote state-of-the-art software verification and validation (SW V&V) methodologies for embedded systems. This partnership, combining virtual platforms and expertise, will extend best practices for embedded software development, debug and test.

Read more here.

Imperas CEO Simon Davidmann Speaks at DVClub Europe

Hear Imperas speak on Software Verification for Low Power and Safety Critical Systems at DVClub Europe, Nov 29, 2016. Where? Online, Bristol, Cambridge and Grenoble.

Read more here.

eSOL RTOS and Debugger Support Available from Imperas for Software Development and Test

eMCOS RTOS Support and eBinder Debugger Integration with Imperas Virtual Platforms

Imperas Software announced their support for the eSOL eMCOS RTOS and eBinder debugger. eSOL is the leading RTOS and embedded software supplier in Japan. This partnership and the new capabilities accelerate embedded software development, debug and test across a variety of markets, including automotive. These solutions are available now.

Highlights:

- Embedded systems developers can get started quickly by using an Imperas Extendable Platform Kit™ (EPK™). An EPK using the

Renesas RH850F1H device and running the eSOL eMCOS real time operating system is available from Imperas.

- Imperas simulators can now use the debugger from the eSOL IDE, eBinder, for fast, intelligent software debug and test.

Read more here.
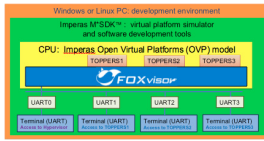
Use a Virtual Platform to Maintain Security
Latest view on security! New article in Embedded Computing, by Larry Lapides.

Security in the IoT ecosystem presents a multi-level challenge incorporating both hardware and software. A pragmatic, cross-functional approach to security in embedded devices and systems is needed, and hypervisors show excellent initial results. Hypervisors are a layer of software that sits between the processor and the operating system and applications, allowing isolation of guest virtual machines, so each can run secure operating systems or applications. Of course, with embedded hypervisors, secure applications, secure communications, and any approach to security, you not only have to develop the approach, you have to test it. Virtual platforms are ideal.

Read more here.

Can You Overcome The Limits Of Scaling?

Article on "Overcoming The Limits Of Scaling Experts at the table, part 1: Complex tradeoffs involving performance, power, cost, packaging, security and reliability come into focus as new markets open for semiconductors and shrinking features becomes increasingly expensive." By Ed Sperling, with Simon Davidmann, in Semiconductor Engineering System-Level Design.

Read more here.

Too Big To Simulate?

Traditional simulation is running out of steam with autonomous vehicles and other complex systems. Now what?" By Ann Steffora Mutschler.

Read more here.

Imperas and SELTECH on Security

SELTECH, a Japan-based developer of hypervisors, joined Imperas at ARM TechCon to discuss and demonstrate their hypervisor-based solutions for safety and security critical embedded systems.
Please contact Imperas or SELTECH for more information.

prpl Foundation at embedded world 2017

Cesare Garlati of prpl will be presenting two papers at embedded world 2017:

- "How We Can Fix Embedded Computing Through an Open Source, Silicon-Layer Approach"
- "How a New Hardware-Based Approach Can Fix Critical Areas of Embedded Computing Security"

OVPsim Release News

OVP: Fast Simulation, Free open source models, Public APIs: Open Virtual Platforms.

A new Imperas and OVP release became available, October 2016.

The Open Virtual Platforms portal is one of the most exciting open source software developments in the embedded software world since GNU created GDB.

- For embedded software developers, virtual platforms are increasingly important, especially for multi-core designs.

The resources on this portal can significantly accelerate your development and test. The next release of OVPsim is expected to be available in January 2017.

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